Course:

CMPE 413: Principles of VLSI Design, Spring 2022. 4 credits.

Course Instructor:

Chintan Patel, Associate Professor, Computer Science & Electrical Engineering

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Office Hours: Mon and Wed, 4:30 - 5:30 pm or by appointment.

Teaching Assistants: (details will be posted on the class webpage)

Text:

Neil H.E. Weste and David Harris, "CMOS VLSI Design: A Circuits and Systems Perspective," Fourth Edition, Addison Wesley (2011)

Supplementary text:

Ken Martin, "Digital Integrated Circuit Design", Oxford University Press (2000).

Jan M. Rabaey, A. Chandrakasan, B. Nikolic "Digital Integrated Circuits, A Design Perspective", Second Edition, Prentice Hall (2003).

Grading:

The distribution of weights for the exams, homeworks and projects is as follows:

Midterm Exam	20%
Final Exam	20%
Labs/Homeworks	25%
Project	30%
Class Participation, Attendance, In-class exercises	5%

No incompletes will be given, except as required by university policy for truly exceptional circumstances. The final exam is cumulative. However, material covered after the second exam will be emphasized. Students are encouraged to participate in class. Any changes to the syllabus will be communicated in class in advance and posted on the webpage.

NOTE: Cheating at any time in this course will cause you to fail the course.

Use the following link for complete description of Undergraduate Student Academic Conduct. Also look at the UMBC Student Handbook for more information.

Undergraduate Student Academic Conduct

Also take a look at the following webpage from the Office of Equity and Inclusion

Office of Equity and Inclusion Standard Syllabus Language

The materials provided at the above two links is part of the syllabus for this course.

Tentative Course Outline:

Week #	Topic
1	Introduction (Lab: Linux/CADENCE setup/tutorial)
1	Basic CMOS Logic Gate Design
2	Transformations: layout/schematic/Boolean expressions
2	CMOS Processing Technology (Lab 1: VHDL)
3	CMOS Processing Technology
3	CMOS Processing Technology
4	MOS Transistors (Lab 2: Schematics and Simulation using SpectreS)
4	MOS Transistors (Lab 3: Layout and Circuit Extraction)
5	MOS Transistors
5	MOS Transistor (Lab 4: Advanced Layout and Simulations)
6	MOS Transistors
6	Technology and Abstractions (Lab 5: Layout and LVS)
7	Midterm Exam (Date subject to change depending on material covered)
7	Exam Review/Performance Estimation (Lab: Project groups and discussion)
8	Performance Estimation (Lab: Project specification/VHDL)
8	TBD
9	TBD (Lab: Project VHDL/Schematic)
9	CMOS Circuit and Logic Design
10	CMOS Circuit and Logic Design (Lab: Project Schematic/Layout)
10	Logical Effort
11	Logical Effort (Lab: Project Layout)
11	CMOS Circuit and Logic Design
12	CMOS Circuit and Logic Design
12	Sequential Circuits
13	Advanced Topics
13	Advanced Topics
14	Advanced Topics (Lab: Final project reports, demos and presentations)
14	Final review
Final week	Final exam

Note: Changes/Additions to this syllabus or schedule will be posted on the class web site. Any syllabus changes will also be communicated in class beforehand.

Class Website