CMPE 413 Lab

LAB Assignment #5 for CMPE 413

Assigned: Fri, Mar 16th
Due: Fri, Apr 1st

Description: Import VHDL code from Lab1, perform layout and run LVS.

- Import the vhdl code that you wrote for the 4-bit ALU circuit in Lab 1 to generate schematics.
- Draw the schematics for the lower level cells and run simulations to verify their functionality.
- Draw the layout for the entire ALU, your layout should be compact and you can design the individual gates as standard cells or a custom layouts with varying heights.
- Extract the layout and run LVS to verify that your layout matches your schematic.

Report Requirements:

1) Print out the top level schematic and layouts for each level of hierarchy. In your report each schematic should be followed by the corresponding layout, until you reach the top level.You can include the description from Lab1 to explain the different levels in your design.
2) Print out the output file (button from main LVS window) showing the status of the schematic to layout verification for the entire circuit. Create a tar file of all your cells that includes all the cell views and submit the tar file along with your a single file for your report. We will run LVS to verify your results.
3) As always, grading will be based on the completeness of your write-up, follow the procedures mentioned in Lab 2 for your write-up.

THE LABS ARE INDIVIDUAL EFFORTS. INSTANCES OF CHEATING WILL RESULT IN YOU FAILING THE COURSE.