Functionality and Robustness

Directivity

Requires a gate to be unidirectional, e.g., changes in an *output level* should not appear at any unchanging input of the same circuit.

Otherwise, noise is generated on gate inputs, affecting *signal integrity*.

Full directivity is never achievable in real circuits, primarily because of gate/channel capacitive coupling.

Fan-in and Fan-out

Increasing the fan-out of a gate can affect its static logic output levels.

From analog amplifiers, ideal is:

- make input resistance of load gates as *large* as possible (to minimize input currents)
- make the output resistance of the driving gate as *small* as possible (to reduce effect of load currents on output voltage)

Functionality and Robustness

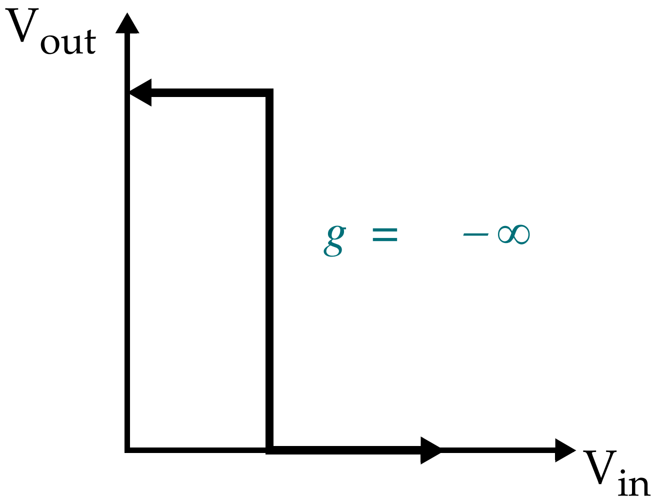
Fan-in and Fan-out

Large fan-outs also degrade the *dynamic* performance of the driving gate.

Similarly, large fan-ins degrade both static and dynamic properties.

The **Ideal Digital Gate** (from the static perspective):

- Has *infinite gain* in the transition region
- *Gate threshold* is located mid logic swing
- *High and low noise margins* equal to half the swing
- *Input/output impedances* are infinity/zero (unlimited fan-out)



Impossible but the static CMOS inverter comes close, as we will see.

Performance

Expresses the computational load that the circuit can manage.

MIPs and FLOPs are used for microprocessors.

Here, we focus on performance as it relates to the **logic design** (as opposed to the architecture).

Performance is expressed as *clock period* or *clock frequency*.

Factors that affect the minimum clock period:

- Propagation delay through the logic
- Time to get data in and out of the registers
- Uncertainty in the clock arrival times (clock skew)

At the core of these factors is performance of the individual gate.

Let t_p represent propagation delay and t_{pHL} and t_{pLH} represent output signal response times.

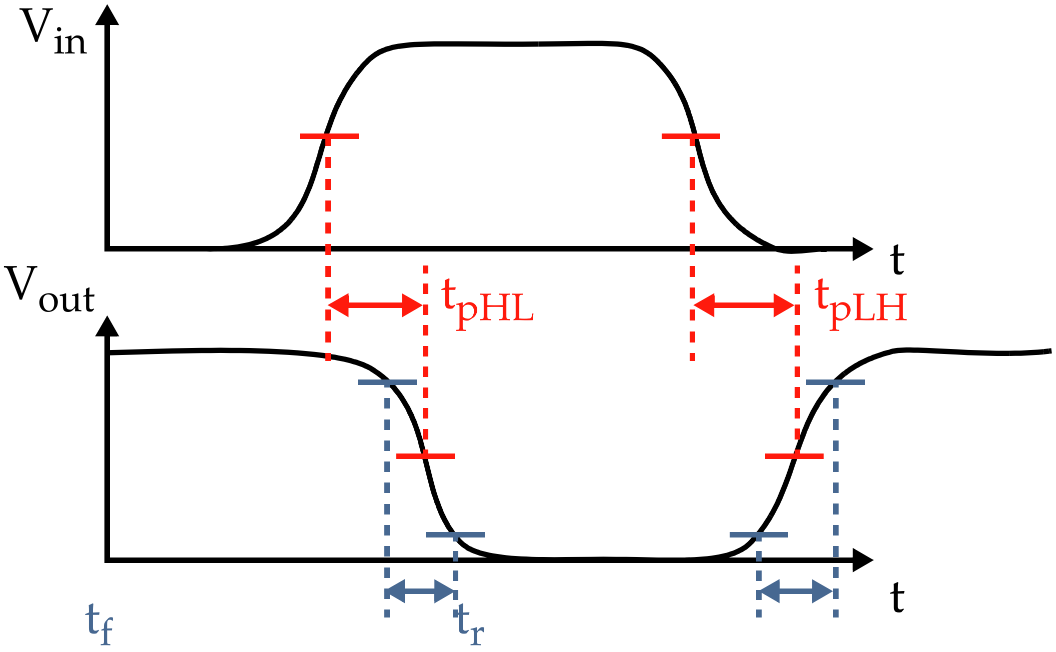
t_{pHL} and t_{pLH} are measured between the **50% points** of the input and output waveforms.

Performance

Define t_p as the **average** of t_{pHL} and t_{pLH} because they are usually not equal:

$$t_p = \frac{t_{pLH} + t_{pHL}}{2}$$

Note that t_p is an **artificial** gate quality metric (used in broader contexts) while t_{pHL} and t_{pLH} are real measures.



Performance

Delay is a function of the **slopes** of the input and output signals of the gate.

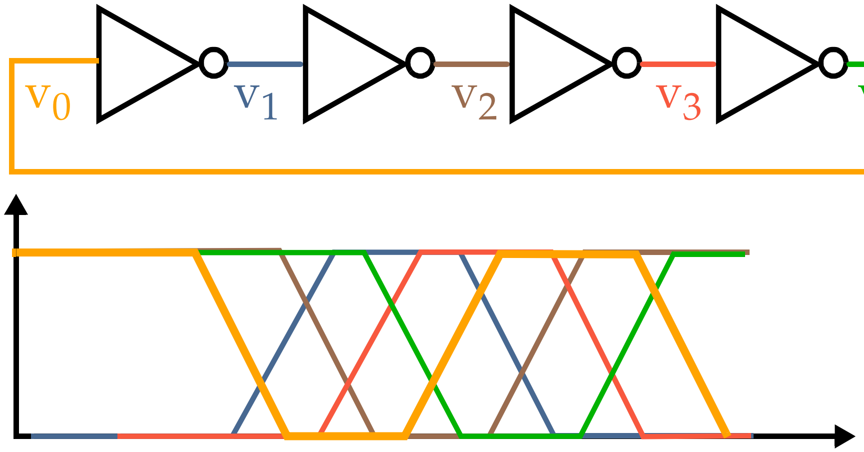
The *uncertainty* in the actual start and stop points is avoided by using the 10% and 90% points.

Note that t_f and t_r are derived from signal **waveforms** and not the gate.

Rise and fall times are affected by:

- Strengths of the driving gate
- The resistive and capacitive load of the driven node

When comparing performance of gates in different technologies or logic styles, load, fan-in and fan-out should **not** be a factor.



Ring oscillator

Performance

The ring oscillator is the *de-facto* standard circuit for **unbiased** delay measurements.

The period T of the oscillation is:

$T = 2 \times t_p \times N$ where N is the # of inverters in the chain.

The factor of 2 indicates that a full cycle consists of both a HL and LH transition.

This equation holds true only for:

$$2Nt_p >> t_f + t_r$$

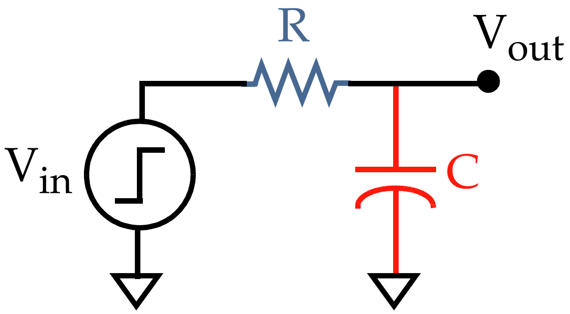
If violated, one wave will overlap with the following, damping the oscillation.

Note that a value for t_p of 20 ps obtained from the ring oscillator does NOT mean that your circuit will operate at 50 GHz!

Real designs have fan-ins and fan-outs > 1, and slow-downs of **50** to **100** over the RO frequency are common.

Performance

The following first-order RC model is often used to model a digital circuit.



Step input produces an exponential transient response.

$$v_{out}(t) = (1 - e^{-t/\tau})V$$

where $\tau = RC$

$V = \text{max value of } V_{in}$

The time to reach the 50% or 90% point are given as:

$$t = \ln(2)\tau = 0.69\tau$$

$$t = \ln(9)\tau = 2.2\tau$$

Power Consumption

Power consumption of a design determines how much **energy** is consumed per operation and how much **heat** is dissipated.

Affect a number of important design decisions:

- Power-supply capacity
- Battery lifetime
- Supply-line sizing
- Packaging
- Cooling requirements

Different dissipation measures are used depending on the design problem:

- **Peak power** (P_{peak}) is important for supply-line sizing.
- **Average power** dissipation (P_{av}) is important for cooling and battery life.

Power Consumption

Both measures are defined by:

$$P_{peak} = i_{peak} V_{supply} = max[p(t)]$$

$$P_{av} = \frac{1}{T}\int_0^T p(t)dt = \frac{V_{supply}}{T}\int_0^T i_{supply}(t)dt$$

Where:

- $p(t)$ is the instantaneous power.
- i_{supply} is the current drawn from the supply voltage V_{supply} over the time interval t in $[0..T]$
- i_{peak} is the maximum value of i_{supply} over that interval.

Dissipation can be further broken down into:

- ❍ **Static**: static conductive paths between the supply rails and leakage currents.
- ❍ **Dynamic**: charging capacitors and temporary current paths.

  It is proportional to the switching frequency.

Power Consumption

Propagation delay and *power consumption* are related.

Delay is determined largely by the speed at which a given amount of **energy** can be stored on gate capacitors.

The faster the energy transfer, the higher the power consumption.

The faster the energy transfer, the faster the gate.

For a given technology and gate topology, the product of power consumption and propagation delay is a constant.

Called the **Power-Delay Product** (PDP).

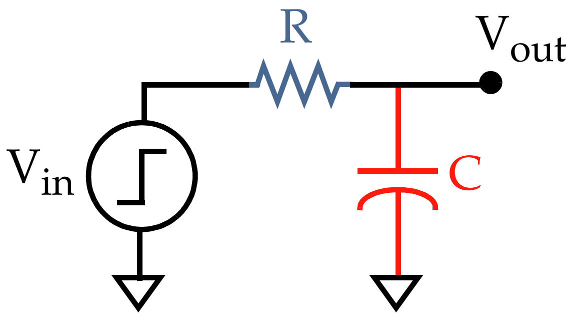
It is the **energy** consumed by the gate *per switching event*, and can be used as a quality measure of the switching device.

Ideal gate is one that is fast and consumes little energy.

The **Energy-Delay** (E-D) product brings them together and is the ultimate measure:

$$\text{E-D} = \text{PDP}^2$$

Power Consumption



The total energy delivered *by the source* is given by:

$$E_{in} = \int_0^{\infty} i_{in}(t)v_{in}(t)dt = V\int_0^{\infty} C\frac{dv_{out}}{\mathrm{dt}}dt = (CV)\int_0^{V} dv_{out} = CV^2$$

Note that the total amount of energy is **independent** of the resistor R.

Energy actually stored *on the capacitor*:

$$E_C = \int_0^{\infty} i_C(t)v_{out}(t)dt = \int_0^{\infty} C\frac{dv_{out}}{\mathrm{dt}}v_{out}dt = C\int_0^{V} v_{out}dv_{out} = \frac{CV^2}{2}$$

The other half is **dissipated as heat** in the resistor.

On the falling edge, the energy on the cap is dissipated in the resistor.