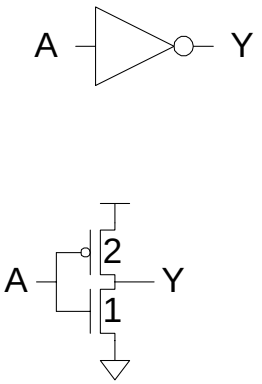
Combinational Circuits

Logical Effort of Compound Gates

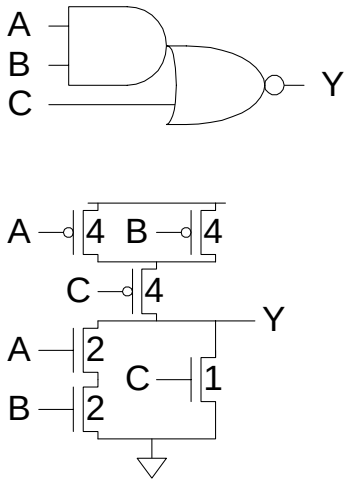
unit inverter



$g_A = 3/3$

$p = 3/3$

AOI21



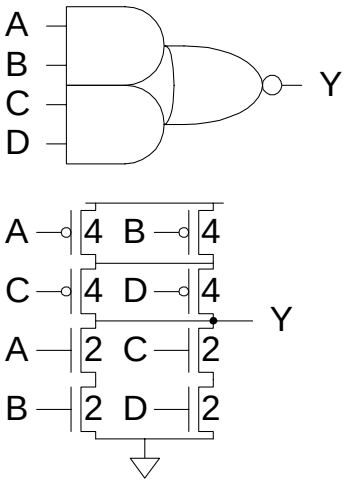
$g_A = 6/3$

$g_B = 6/3$

$g_C = 5/3$

$p = 7/3$

AOI22



$g_A = 6/3$

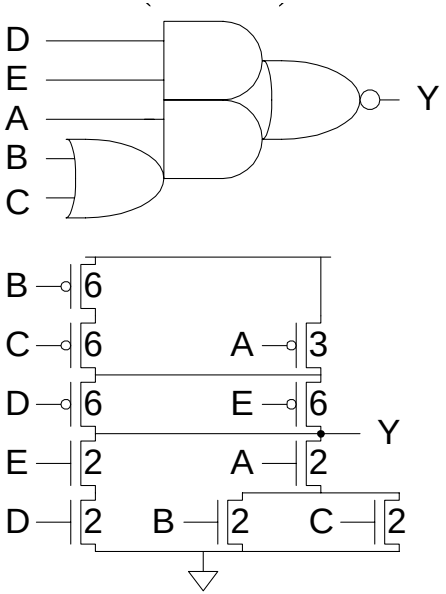
$g_B = 6/3$

$g_C = 6/3$

$g_D = 6/3$

$p = 12/3$

Complex AOI



$g_A = 5/3$

$g_B = 8/3$

$g_C = 8/3$

$g_D = 8/3$

$g_E = 8/3$

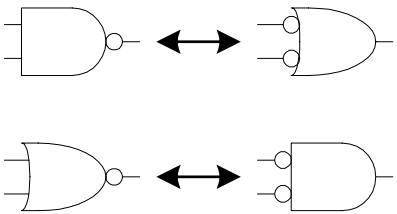
$p = 16/3$

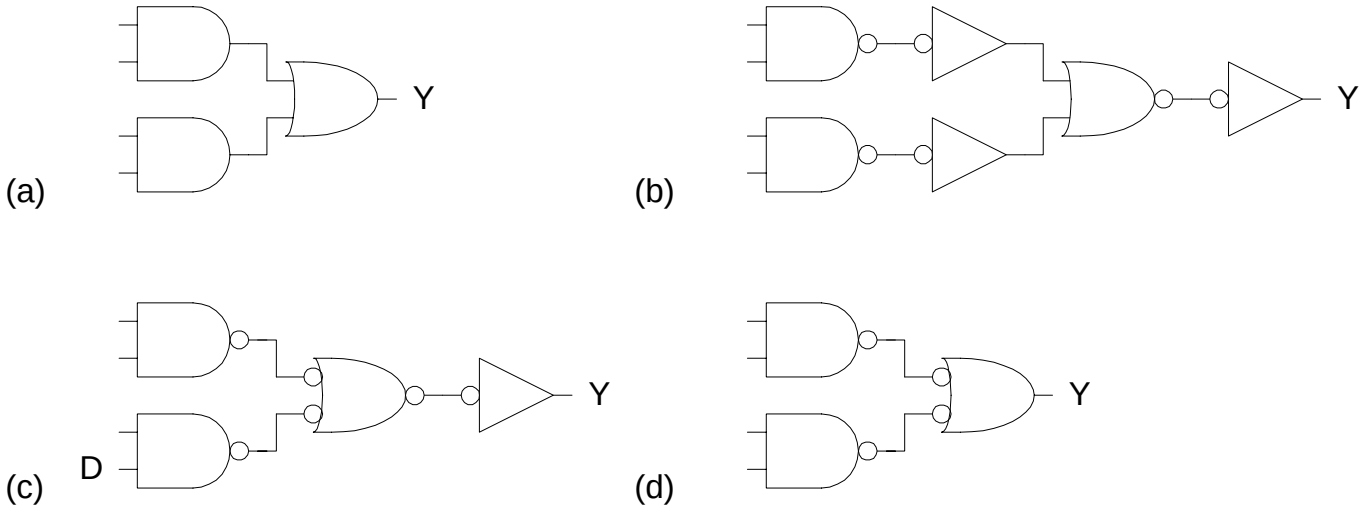
Combinational Circuits

Bubble Pushing

- Start with network of AND/OR gates
- Convert to NAND/NOR + inverters
- Push bubbles around to simplify logic

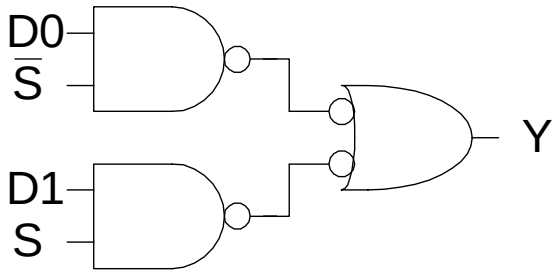
DeMorgan's Law

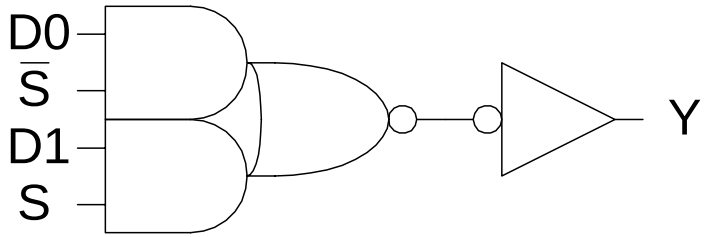




Combinational Circuits

Multiplexer example: Estimate the delay of NAND and compound gate designs of a mux with maximum capacitance of 16 units on each input and an output load of 160 units





$H = 160/16 = 10$
$B = 1$
$N = 2$

$P = 2 + 2 = 4$

$G = (4/3) * (4/3) = 16/9$

$F = GBH = 160/9$

$\hat{f} = \sqrt[N]{F} = 4.2$

$D = N\hat{f} + P = 12.4\tau$

$P = 4 + 1 = 5$

$G = (6/3) * (1) = 2$

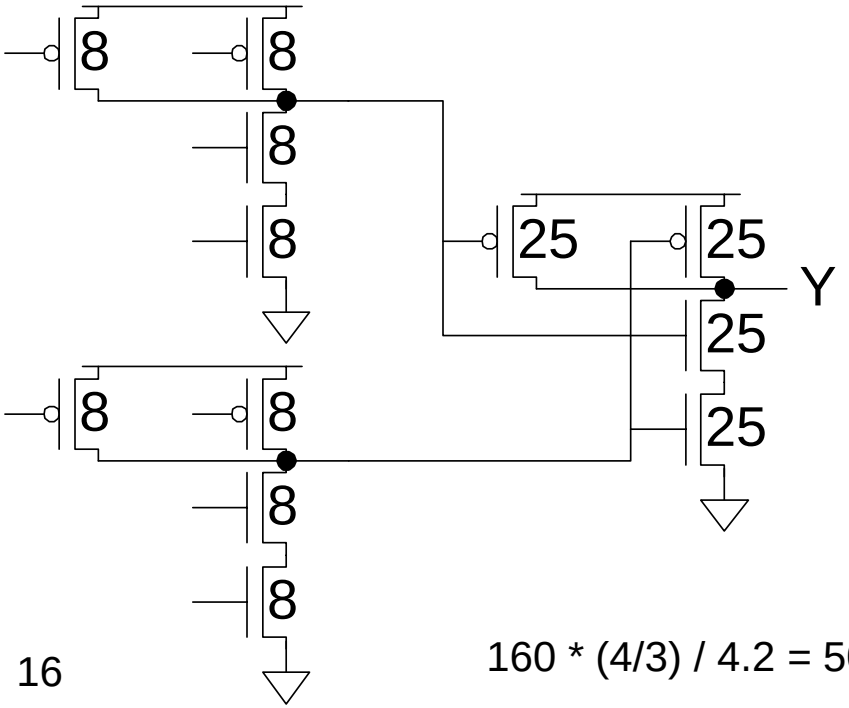
$F = GBH = 20$

$\hat{f} = \sqrt[N]{F} = 4.5$

$D = N\hat{f} + P = 14\tau$

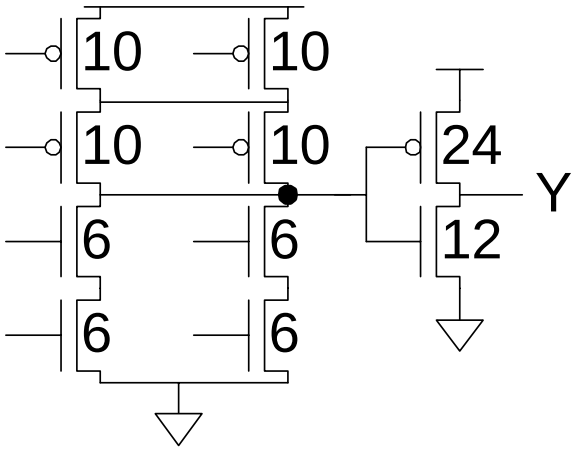
Combinational Circuits

Example (contd.): Annotate transistor sizes to achieve the above delays



16

160 * (4/3) / 4.2 = 50



16

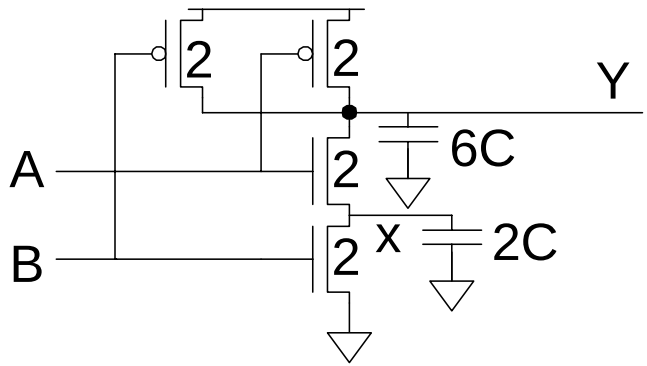
160 * 1 / 4.5 = 36

Input Ordering

We were using a very simple delay model

Let's calculate the parasitic delay for Y falling, considering input arrival times i.e.

- If A arrives latest?
- If B arrives latest?



With A arriving the latest the delay is 2τ

However with B arriving the latest the delay is 2.33τ

Outer input is the one closest to the supply rail (B)

Inner input is the closest to the output (A)

If input arrival times are known, connect the latest input to the inner terminal

Asymmetric Gates

Asymmetric gates favor one *input* over the other

E.g. Suppose input A is the most critical

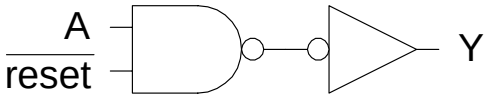
- Use smaller transistor on A (less C)
- Boost size of non-critical input
- This keeps the total resistance the same

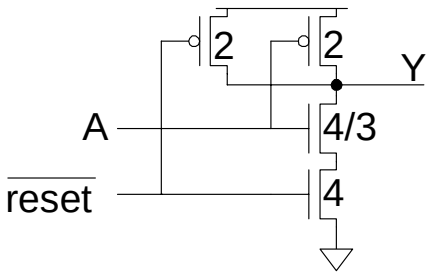
$g_A = 10/9$

$g_{RESET} = 2$

$g_{TOTAL} = g_A + g_{RESET} = 28/9$

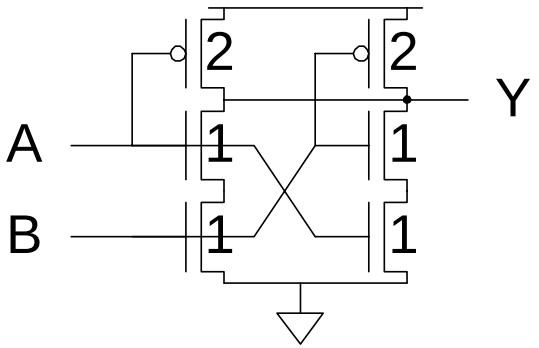
Asymmetric gate approaches g=1 on critical input but total logical effort goes up





Symmetric gates

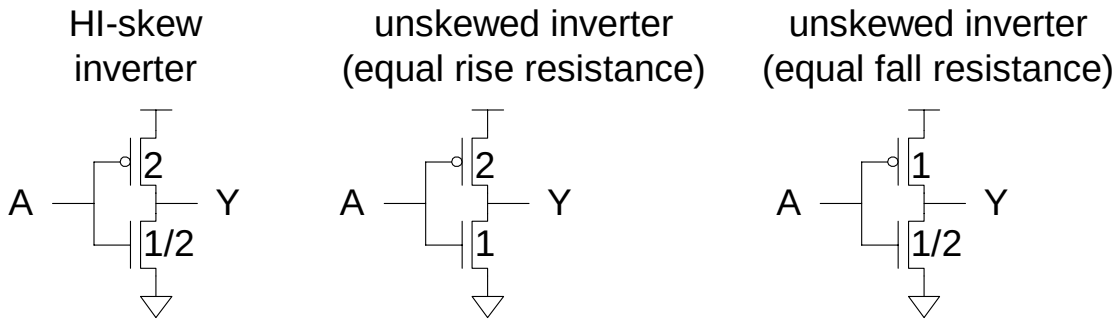
Inputs can be made perfectly symmetric



Skewed Gates

Skewed gates favor one *edge* over the other

Ex: Rising output of the inverter is the most critical
Downsize the non-critical NMOS transistor



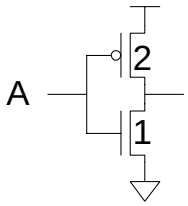
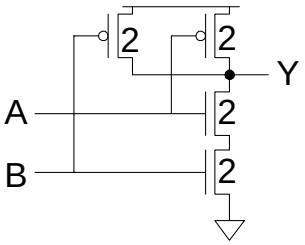
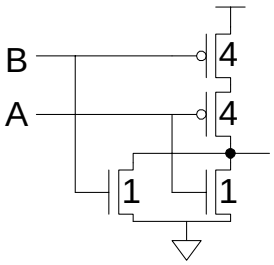
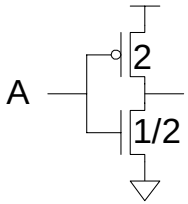
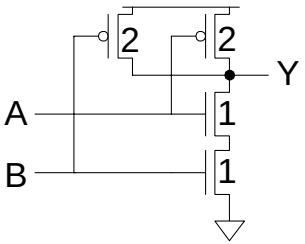
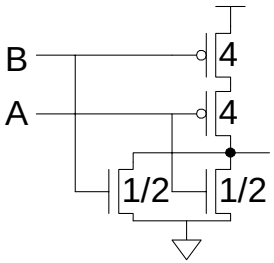
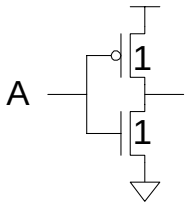
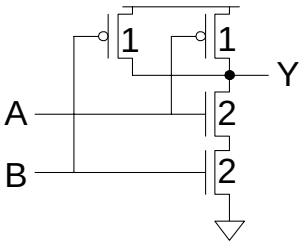
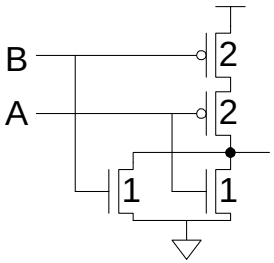
Definition: Logical effort of a skewed gate for a particular transition is the ratio of the input capacitance of that gate to the input capacitance of an unskewed inverter delivering the same output current for the same transition

$g_u = 2.5/3 = 5/6$, $g_d = 2.5/1.5 = 5/3$

Skewed gates reduce size of non-critical transistors

Logical effort is smaller for preferred direction but larger for the other direction

Skewed Gates

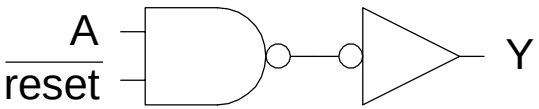
	Inverter	NAND2	NOR2
unskewed	 $g_u = 1$ $g_d = 1$ $g_{avg} = 1$	 $g_u = 4/3$ $g_d = 4/3$ $g_{avg} = 4/3$	 $g_u = 5/3$ $g_d = 5/3$ $g_{avg} = 5/3$
HI-skew	 $g_u = 5/6$ $g_d = 5/3$ $g_{avg} = 5/4$	 $g_u = 1$ $g_d = 2$ $g_{avg} = 3/2$	 $g_u = 3/2$ $g_d = 3$ $g_{avg} = 9/4$
LO-skew	 $g_u = 4/3$ $g_d = 2/3$ $g_{avg} = 1$	 $g_u = 2$ $g_d = 1$ $g_{avg} = 3/2$	 $g_u = 2$ $g_d = 1$ $g_{avg} = 3/2$

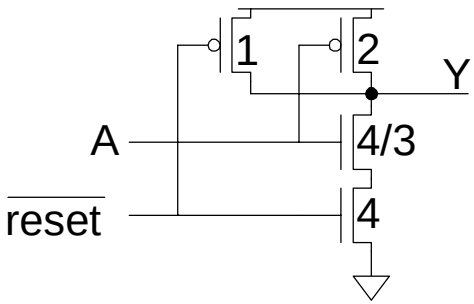
Asymmetric Skew

Combine asymmetric and skewed gates

Downsize non-critical transistors on unimportant input

Reduce parasitic delay for critical input



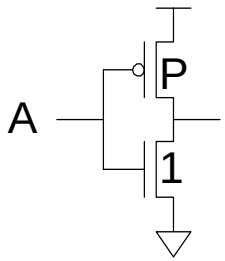


Best P/N Ratio

We have been selecting the P/N ratio to obtain unit rise and fall resistance (2-3 for inverter)

Alternative: choose ratio for least average delay

Eg: Inverter delay, driving an identical inverter (μ = P/N ratio)



$t_{pdf} = (P + 1)$

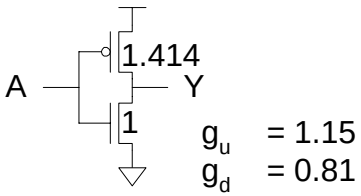
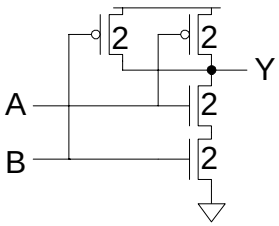
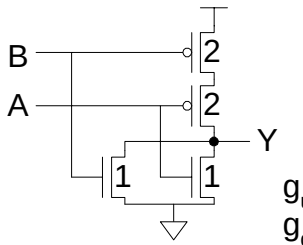
$t_{pdr} = (P + 1)\ (\mu/P)$

$t_{pd} = (P + 1)\ (1 + \mu/P) / 2 = (P + 1 + \mu + \mu/P) / 2$

Differentiate wrt P, least delay for $P = \sqrt{\mu}$

In general, best P/N ratio is sqrt of that giving equal delay

- Only improves average delay slightly for inverters
- But significantly reduces both area and power

	Inverter	NAND2	NOR2
fastest P/N ratio			
	g_u = 1.15 g_d = 0.81 g_{avg} = 0.98	g_u = 4/3 g_d = 4/3 g_{avg} = 4/3	g_u = 2 g_d = 1 g_{avg} = 3/2

Combination Circuit Observations

For speed:

- NAND vs. NOR
- Many simple stages vs. fewer high fan-in stages
- Latest-arriving input

For area and power:

- Many simple stages vs. fewer high fan-in stages