## DC Response

***DC Response:*** $V_{out}$ vs. $V_{in}$ for a gate

- Ex: Inverter

  When $V_{in} = 0$ -> $V_{out} = V_{DD}$

  When $V_{in} = 1$ -> $V_{out} = 0$

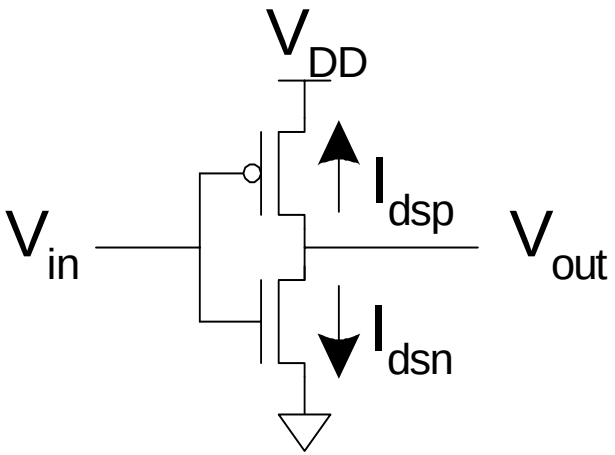
  In between, $V_{out}$ depends on transistor size and current.

  By KCL, must settle such that $\mathbf{I_{dsn} = |I_{dsp}|}$

  Could solve analytically or using simulations but a graphical solution is easier.

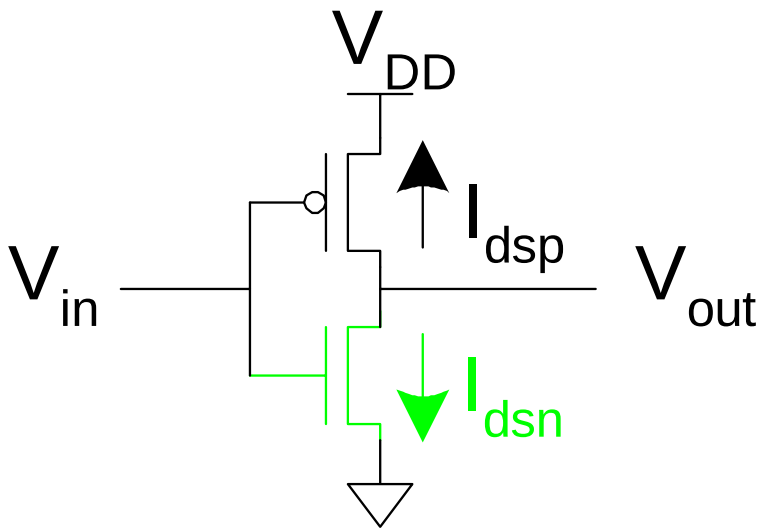
  From previous analysis, we know that current depends on the region of operation.

  So we need to the region of operation for all values of $V_{in}$ and $V_{out}$.



## NMOS Operation

| Cutoff | Linear | Saturation |
|---|---|---|
| $V_{gsn} < V_{tn}$<br>$V_{in} < V_{tn}$ | $V_{gsn} > V_{tn}$<br>$V_{in} > V_{tn}$<br>$V_{dsn} < V_{gsn} - V_{tn}$<br>$V_{out} < V_{in} - V_{tn}$ | $V_{gsn} > V_{tn}$<br>$V_{in} > V_{tn}$<br>$V_{dsn} > V_{gsn} - V_{tn}$<br>$V_{out} > V_{in} - V_{tn}$ |



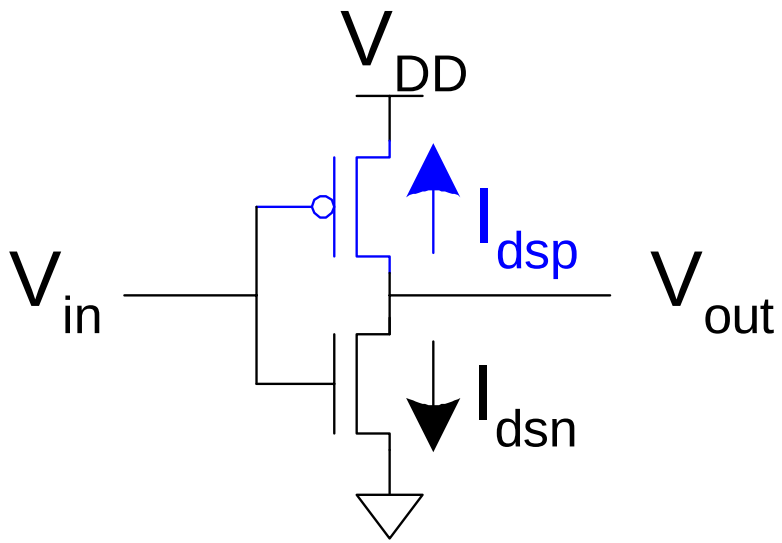

$V_{gsn} = V_{in}$

$V_{dsn} = V_{out}$

$V_{tn} > 0$

## PMOS Operation

| Cutoff | Linear | Saturation |
|---|---|---|
| $V_{gsp} > V_{tp}$<br>$V_{in} > V_{DD} + V_{tp}$ | $V_{gsp} < V_{tp}$<br>$V_{in} < V_{DD} + V_{tp}$<br>$V_{dsp} > V_{gsp} - V_{tp}$<br>$V_{out} > V_{in} - V_{tp}$ | $V_{gsp} < V_{tp}$<br>$V_{in} < V_{DD} + V_{tp}$<br>$V_{dsp} < V_{gsp} - V_{tp}$<br>$V_{out} < V_{in} - V_{tp}$ |

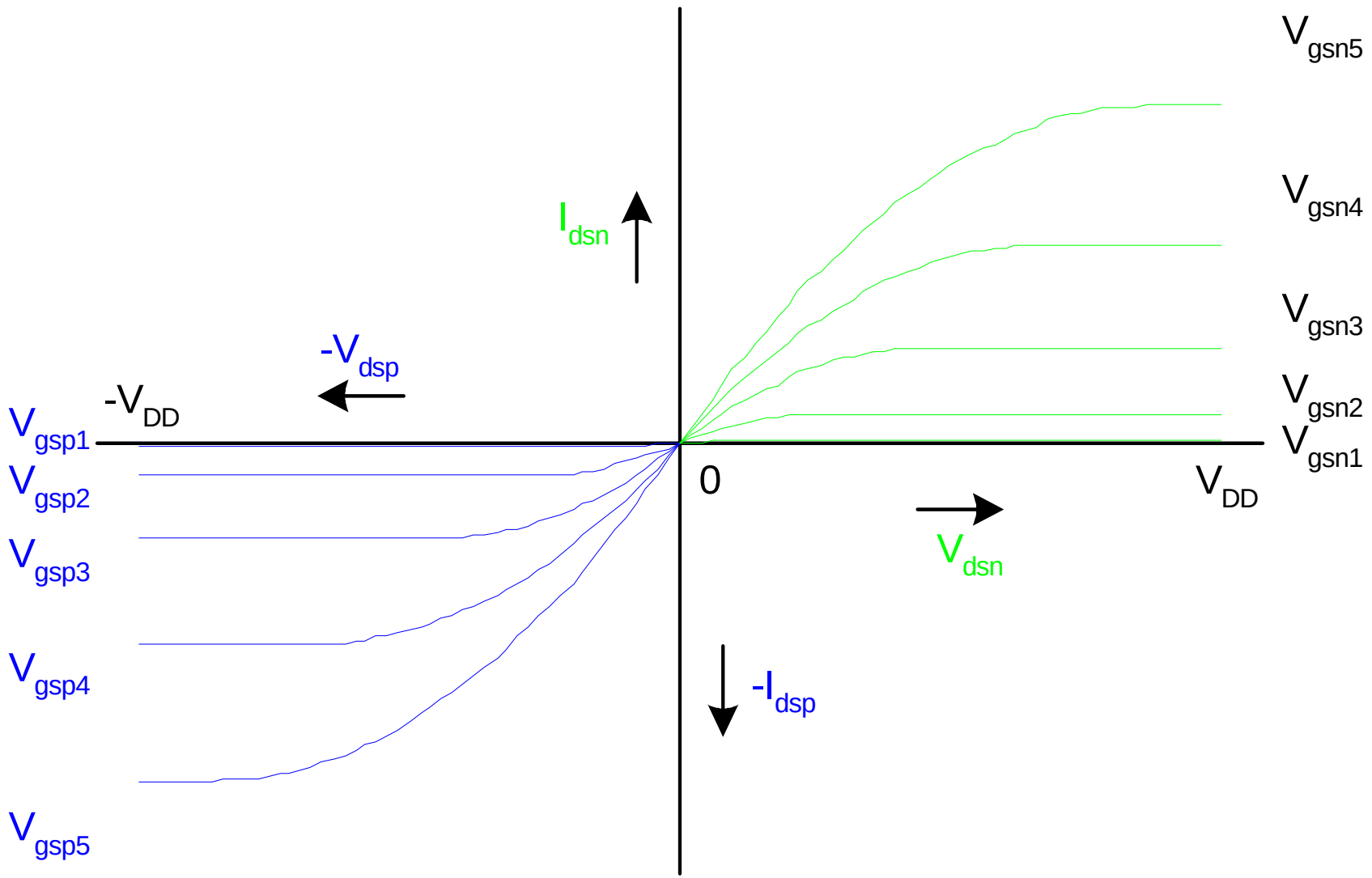



$V_{gsp} = V_{in} - V_{DD}$

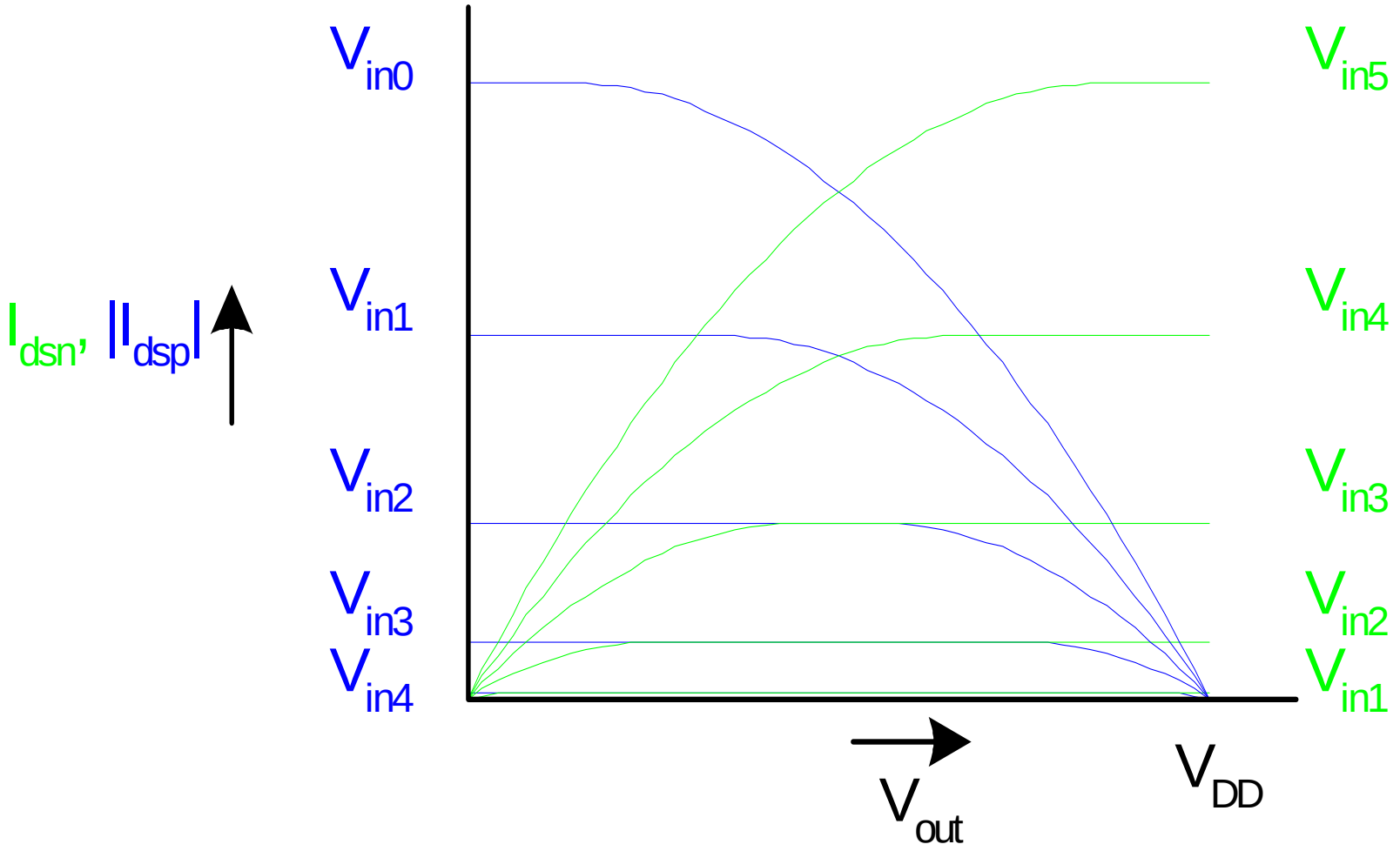
$V_{dsp} = V_{out} - V_{DD}$

$V_{tp} < 0$

## I-V Characteristic



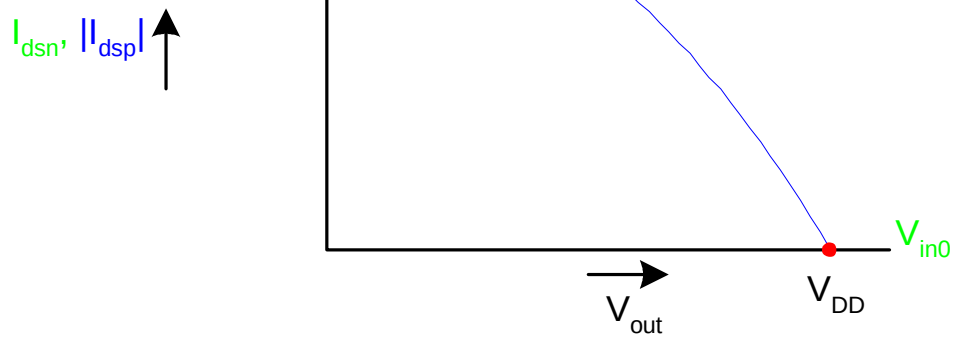
## *Current vs. $V_{out}$, $V_{in}$*



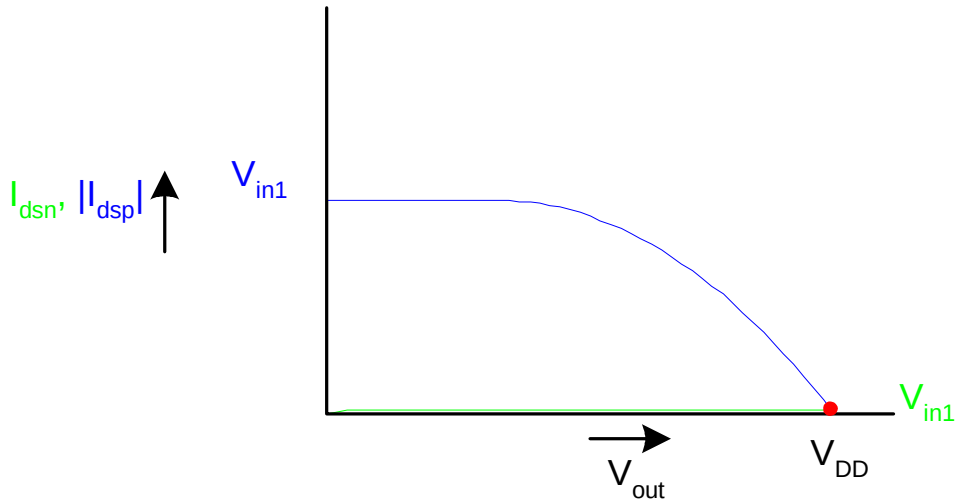
## Load Line Analysis

For a given $V_{in,}$ Plot $I_{dsn}$, $I_{dsp}$ vs. $V_{out}$. ($V_{out}$ values where |currents| are equal)

$V_{in} = 0$

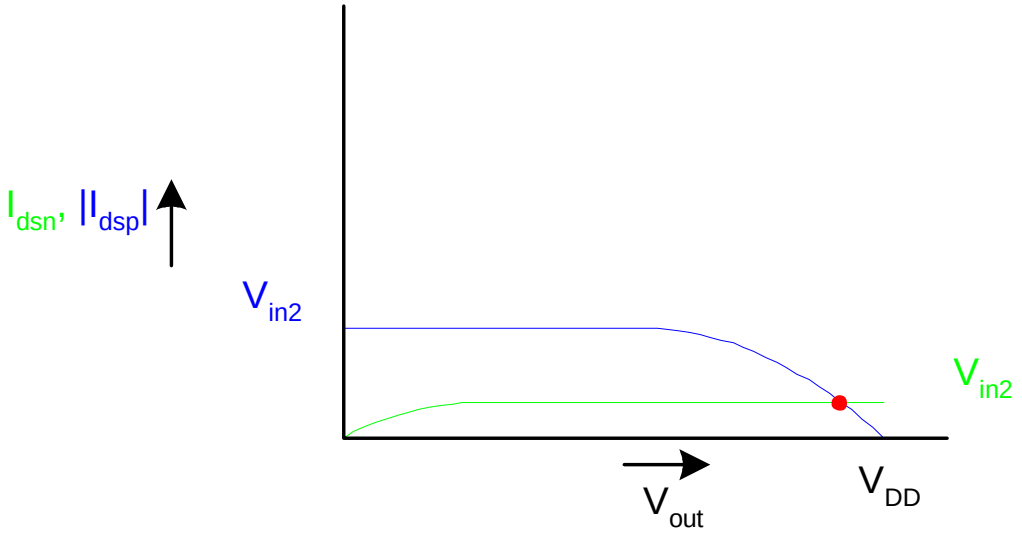



$V_{in} = 0.2\ V_{DD}$

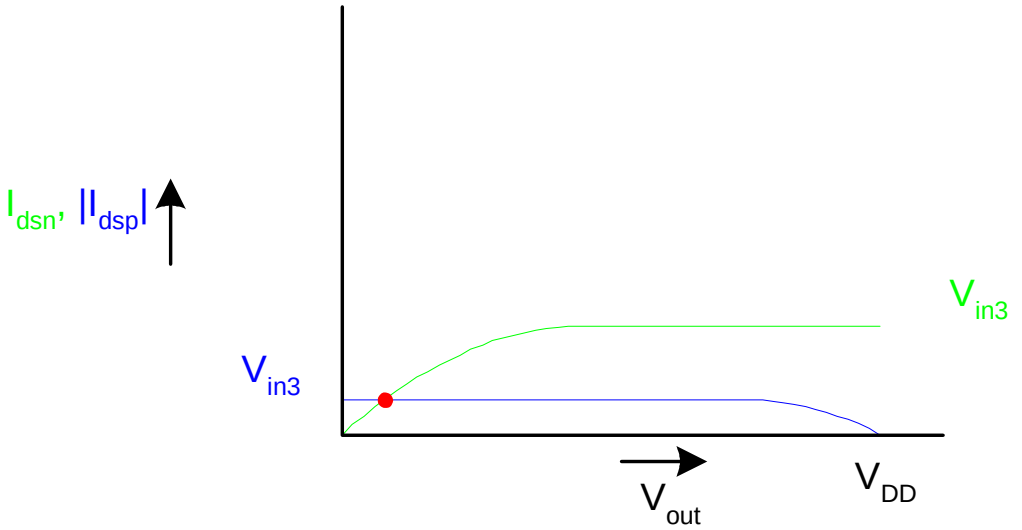


## Load Line Analysis

$V_{in} = 0.4\ V_{DD}$

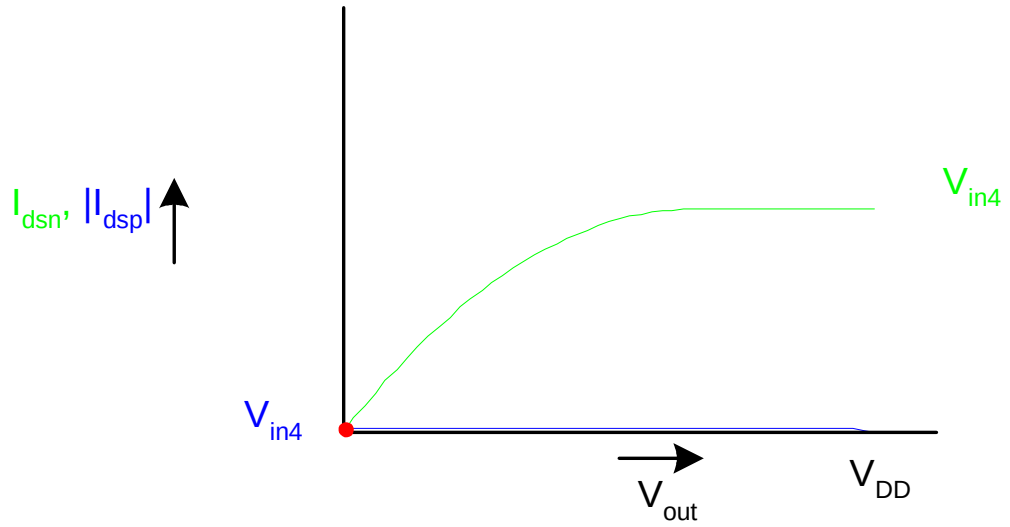



$V_{in} = 0.6\ V_{DD}$

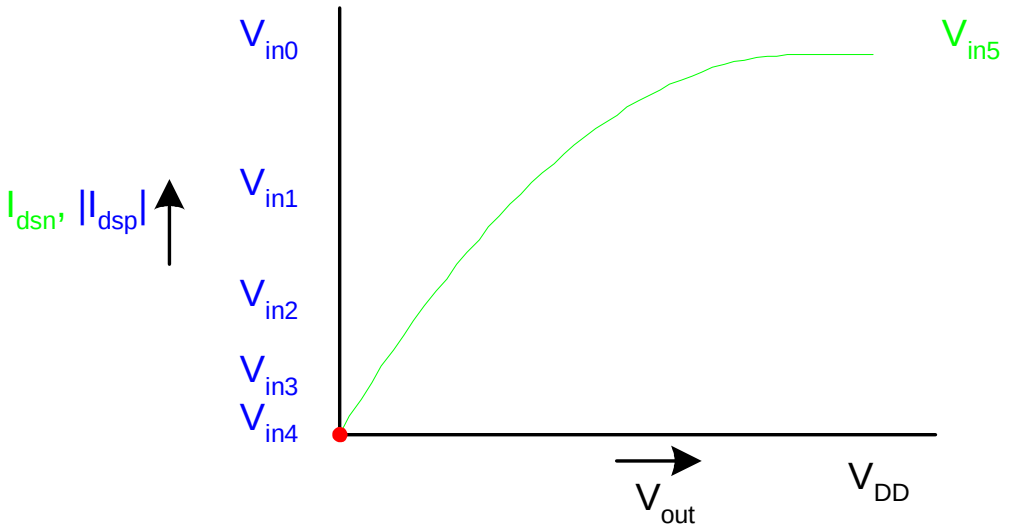


## Load Line Analysis

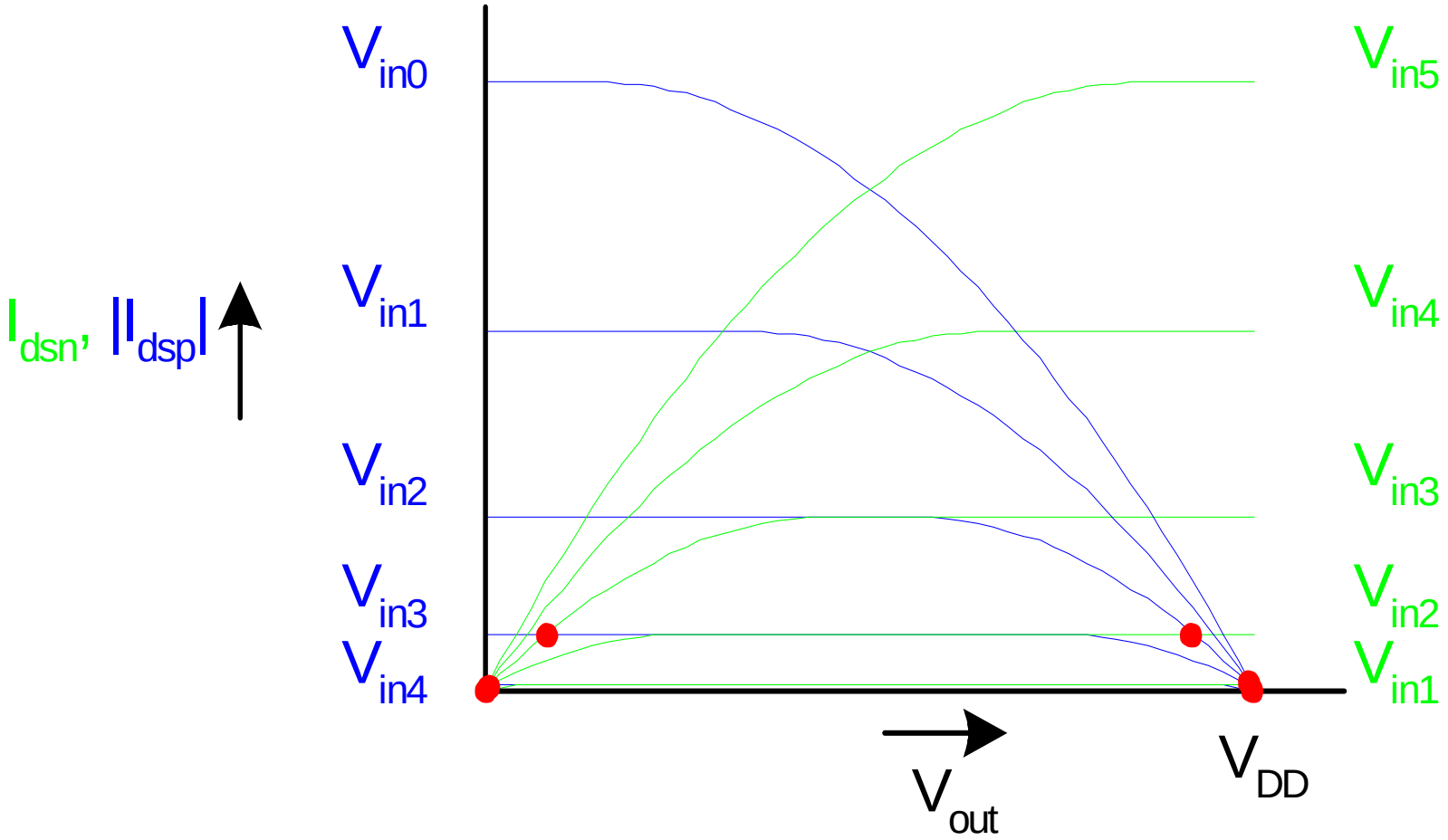
$V_{in} = 0.8\ V_{DD}$



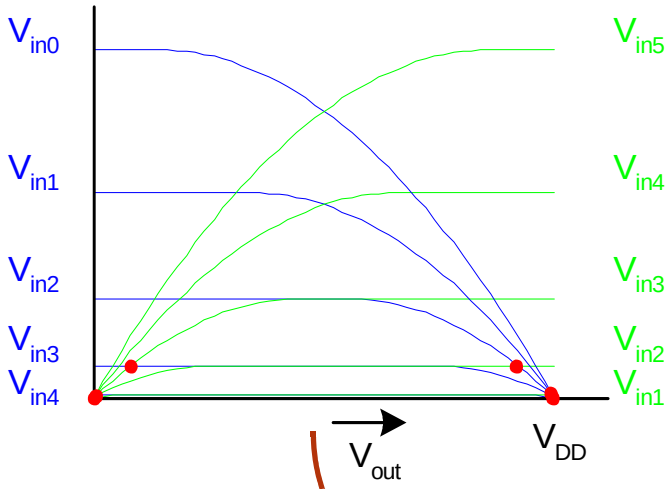

$V_{in} = V_{DD}$

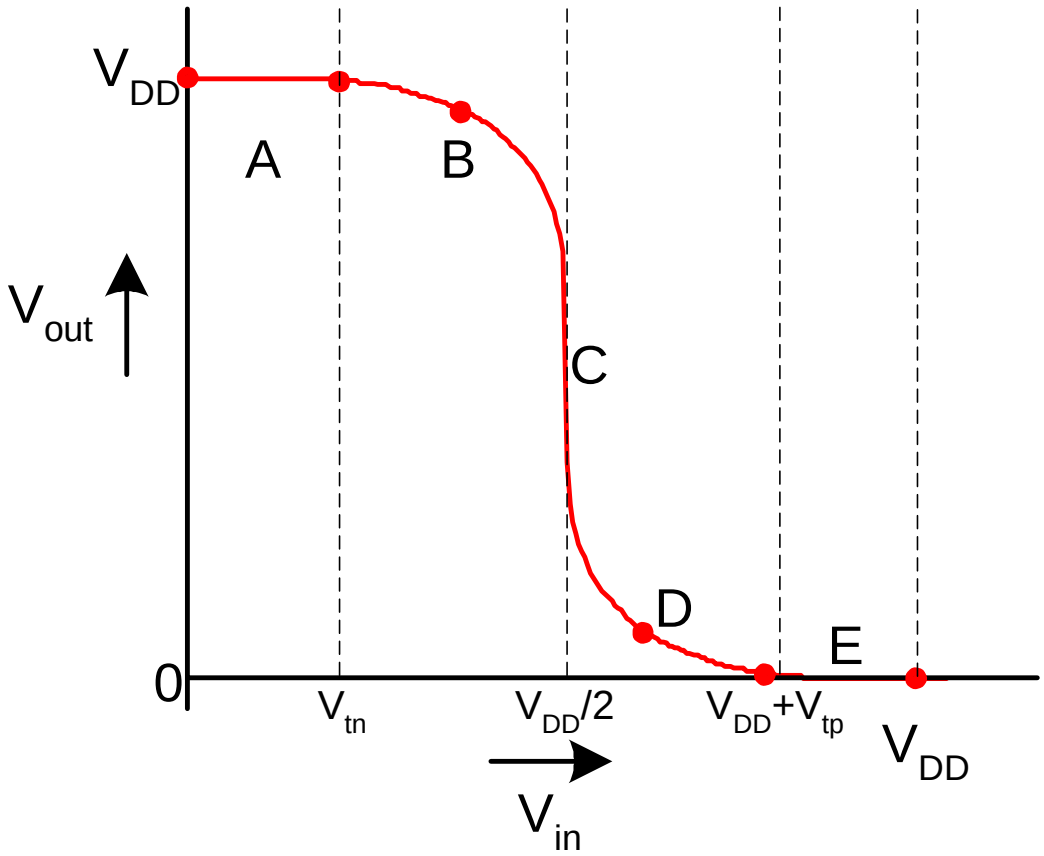


## Load Line Summary



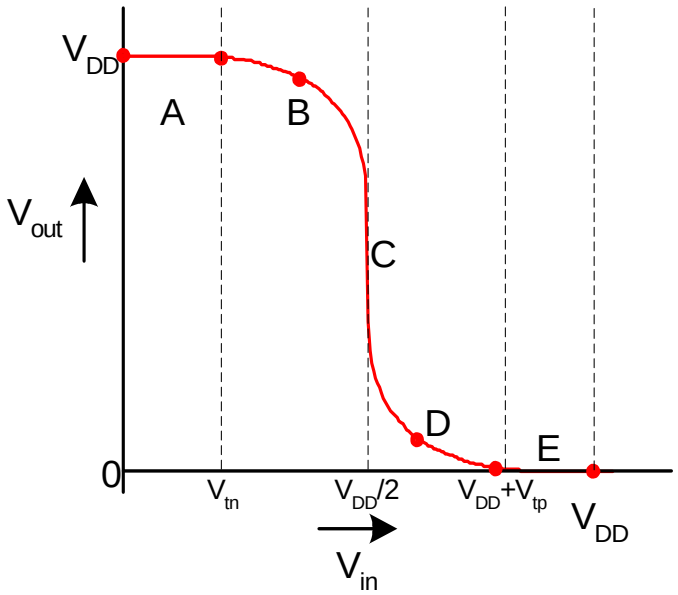
## DC Transfer Curve

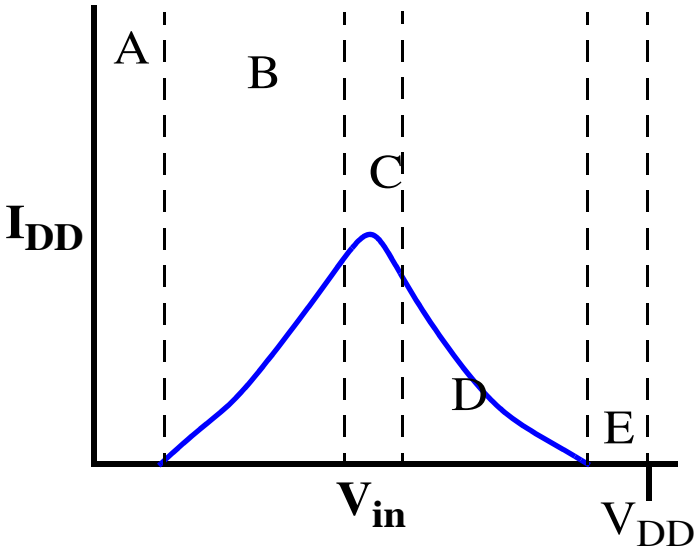


## Operating Regions and Supply Current

| Region | NMOS | PMOS |
|---|---|---|
| A | Cutoff | Linear |
| B | Saturation | Linear |
| C | Saturation | Saturation |
| D | Linear | Saturation |
| E | Linear | Cutoff |

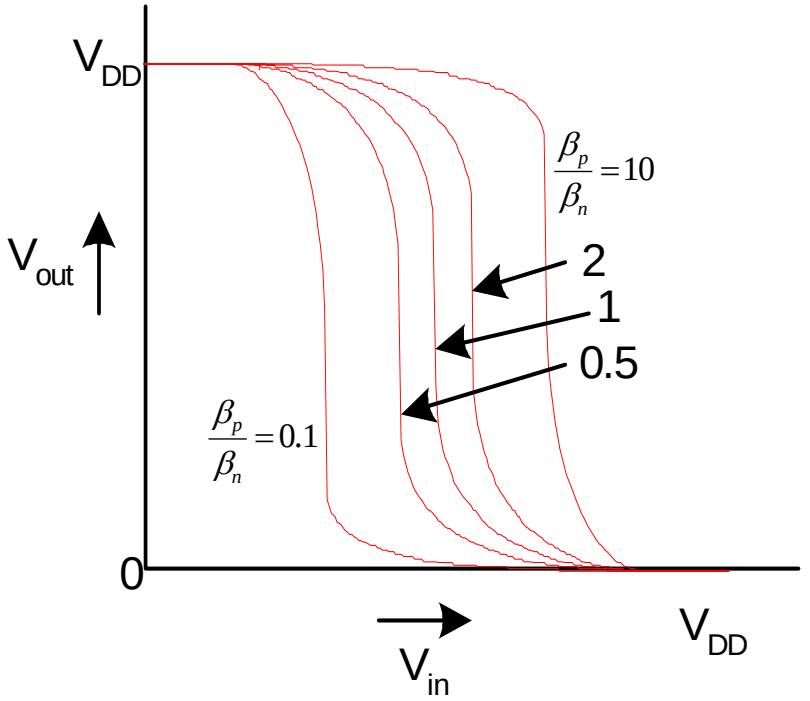



Supply current $I_{DD}$ vs. $V_{in}$.

## Beta Ratios

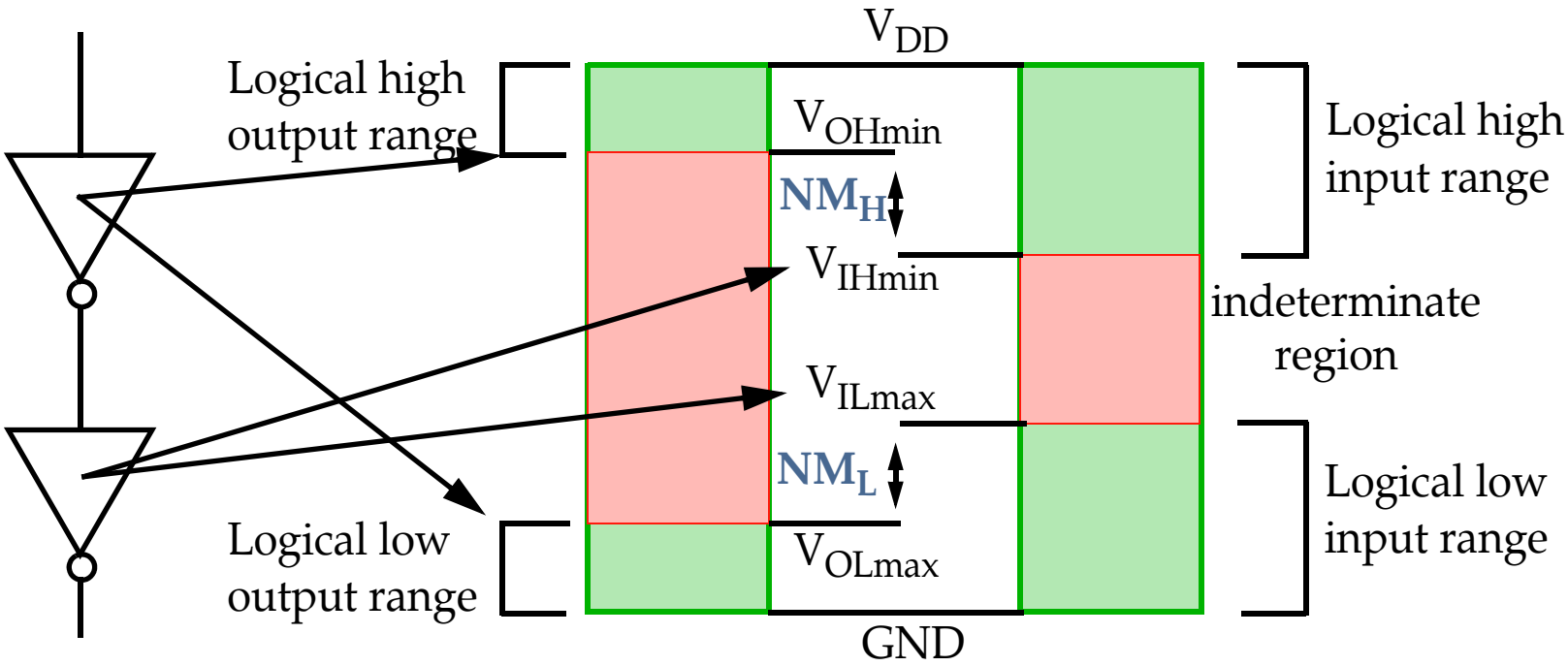
- If $\beta_p \neq \beta_n$, switching point will move from $V_{DD}/2$.
- Called *skewed* gate
- Other gates: Collapse into equivalent inverter
- Curves shift, but the output transition in the C region still remains sharp
- Therefore, beta ratios don't affect switching performance
- With equal beta values the time required to charge or discharge the out-put load capacitance is equal
- Results in equal rise and fall times



## Noise Margins

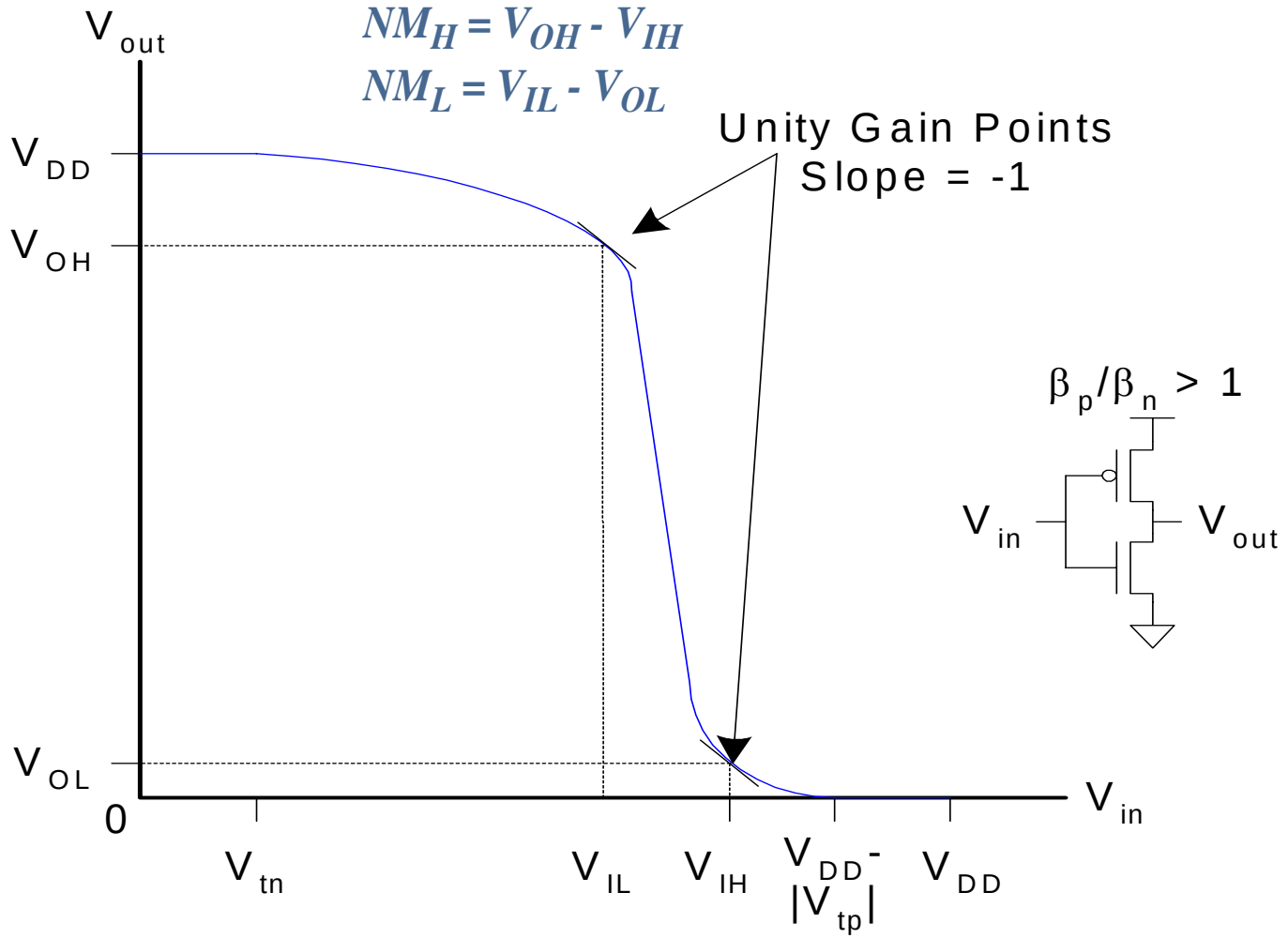
- A parameter that determines the maximum *noise* voltage on the input of a gate that allows the output to remain stable.
- Two parameters, Low noise margin ($NM_L$) and High noise margin ($NM_H$).

  $NM_L$ = difference in magnitude between the max LOW output voltage of the driving gate and max LOW input voltage recognized by the driven gate. $NM_H$ is similar for high voltage input and output range.

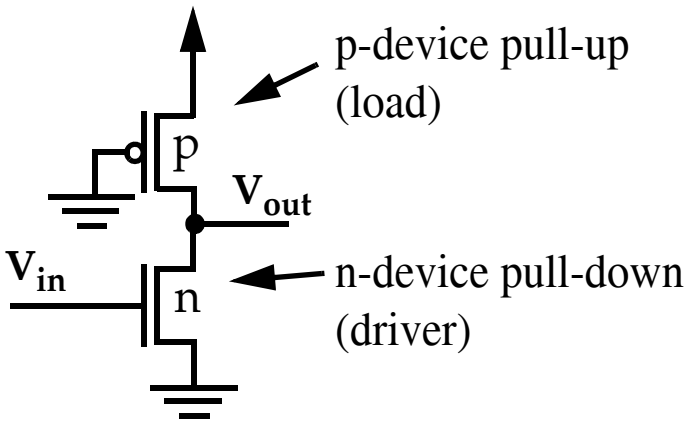


## Logic Levels

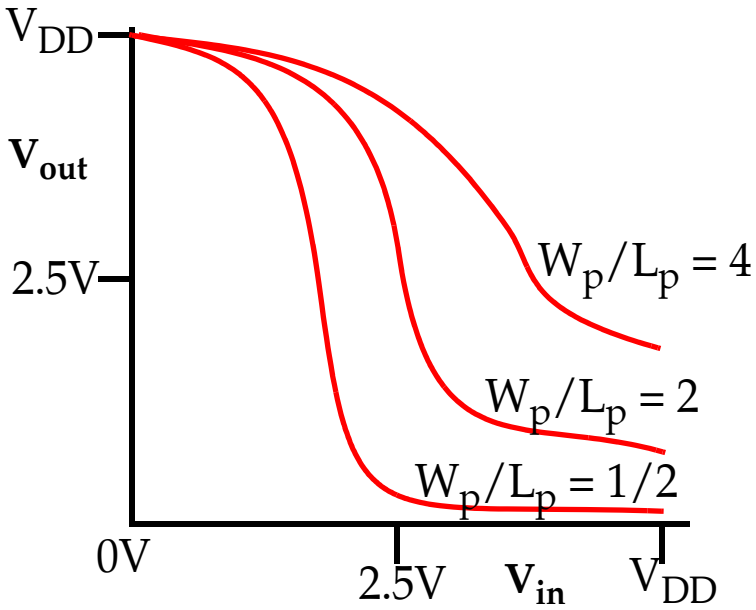
To maximize noise margins, select logic levels at unity gain points of DC transfer characteristics



## *Pseudo-nMOS Inverter*




When driver is on, steady-state current flows - not a good choice for low-power circuits.



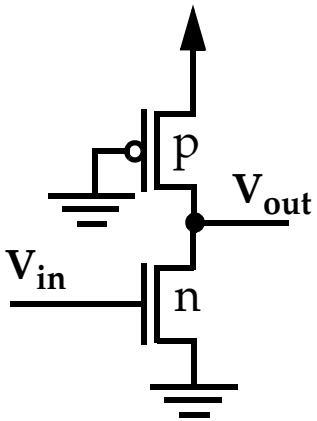

Therefore, the shape of the transfer characteristic and the $V_{OL}$ of the inverter is affected by the ratio $\frac{\beta_n}{\beta_p}$.

In general, the low noise margin is considerably worse than the high noise margin for Pseudo-nMOS.

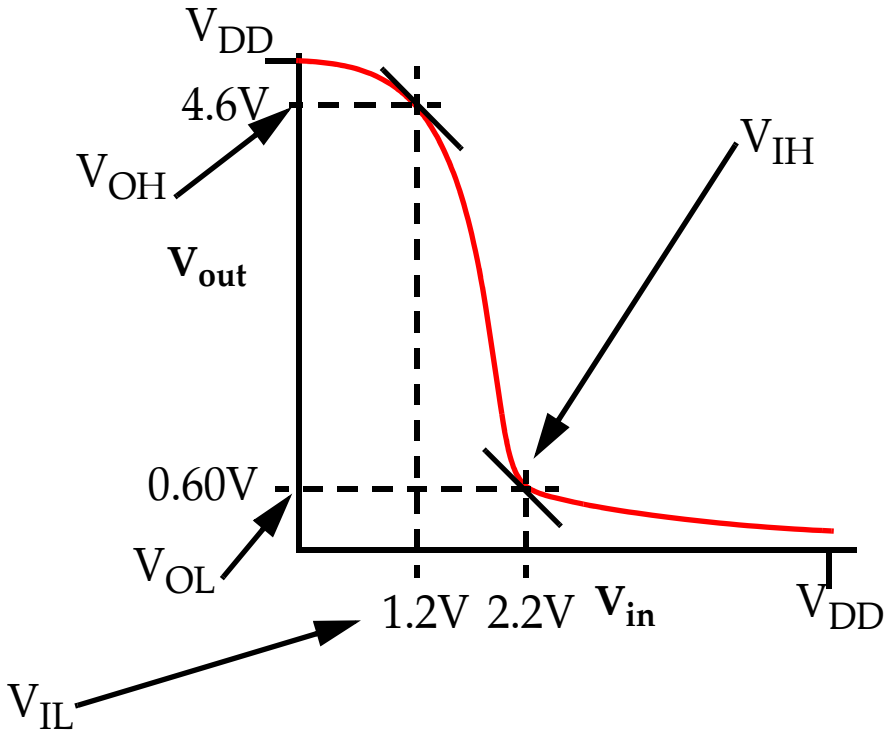
Pseudo-nMOS was popular for high-speed circuits, static ROMs and PLAs.

## *Pseudo-nMOS*

Example: Calculation of noise margins:




Pseudo-nMOS inverter




$NM_H = V_{OH} - V_{IH} = 4.6V - 2.2V = 2.4V$

$NM_L = V_{IL} - V_{OL} = 1.2V - 0.60V = 0.60V$ (This is quite a bit worse than $NM_H$)

## Transient Response

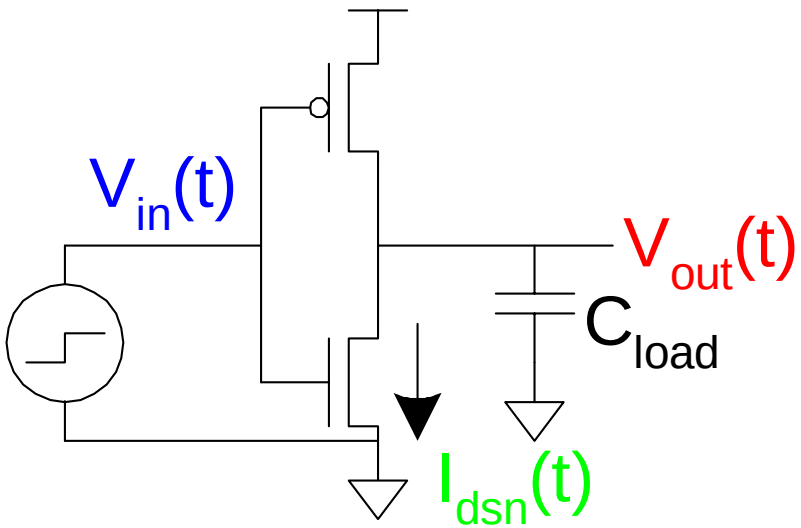
DC analysis tell us $V_{out}$ if $V_{in}$ is constant.

Transient analysis tells us $V_{out}(t)$ if $V_{in}(t)$ changes.

Requires solving differential equations

Input is usually considered to be a step or ramp from $V_{DD}$ to 0 or vice versa.

*Step response of inverter driving a capacitive load*

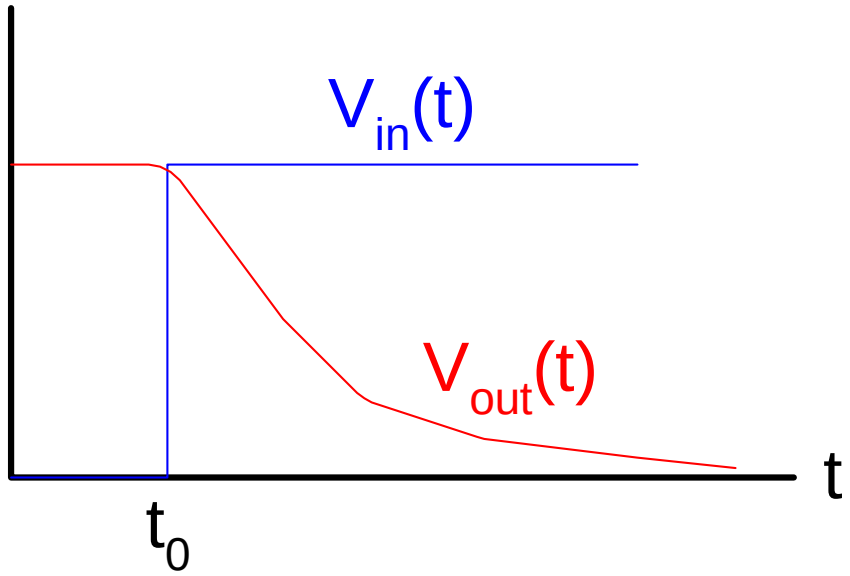


## Inverter Step Response

$$V_{in}(t) = u(t - t_0)V_{DD}$$

$$V_{out}(t < t_0) = V_{DD}$$

$$\frac{dV_{out}}{dt} = \frac{I_{dsn}(t)}{C_{load}}$$




$$I_{dsn}(t) = \begin{cases} 0 & t < t_0 \\ \frac{\beta}{2}(V_{DD} - V)^2 & V_{out} > V_{DD} - V_t \\ \beta(V_{DD} - V_t - V_{out}(t)/2)V_{out}(t) & V_{out} < V_{DD} - V_t \end{cases}$$