MOS: Metal Oxide Semiconductor

Transistors are built on a **Silicon** (semiconductor) substrate.

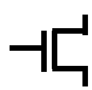
Pure silicon has no free carriers and conducts poorly.

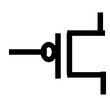
Dopants are added to increase conductivity: extra electrons (**n-type**) or extra holes (**p-type**)

MOS structure created by superimposing several layers of conducting, insulating and transistor-forming materials.

Metal gate has been replaced by polysilicon or poly in modern technologies.

There are two types of MOS transistors:

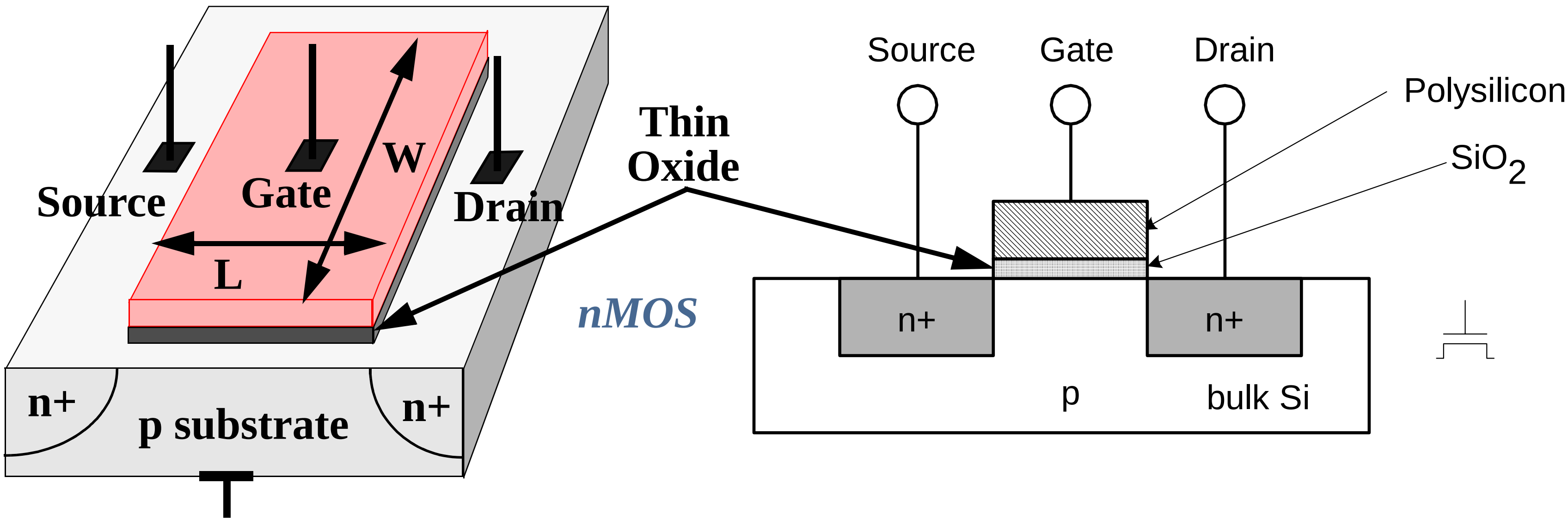
nMOS  : Negatively doped silicon, rich in electrons.

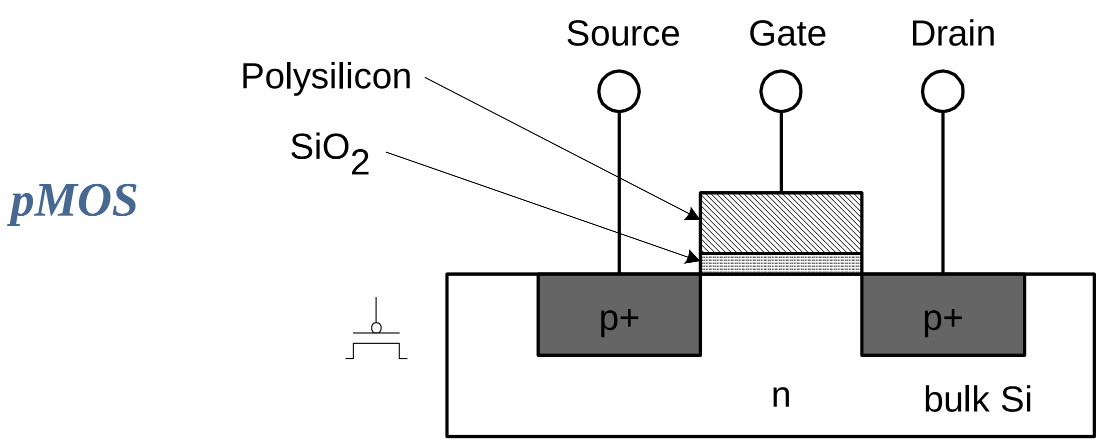
pMOS  : Positively doped silicon, rich in holes.

CMOS: Both type of transistors are used to construct any gate.

nMOS and pMOS

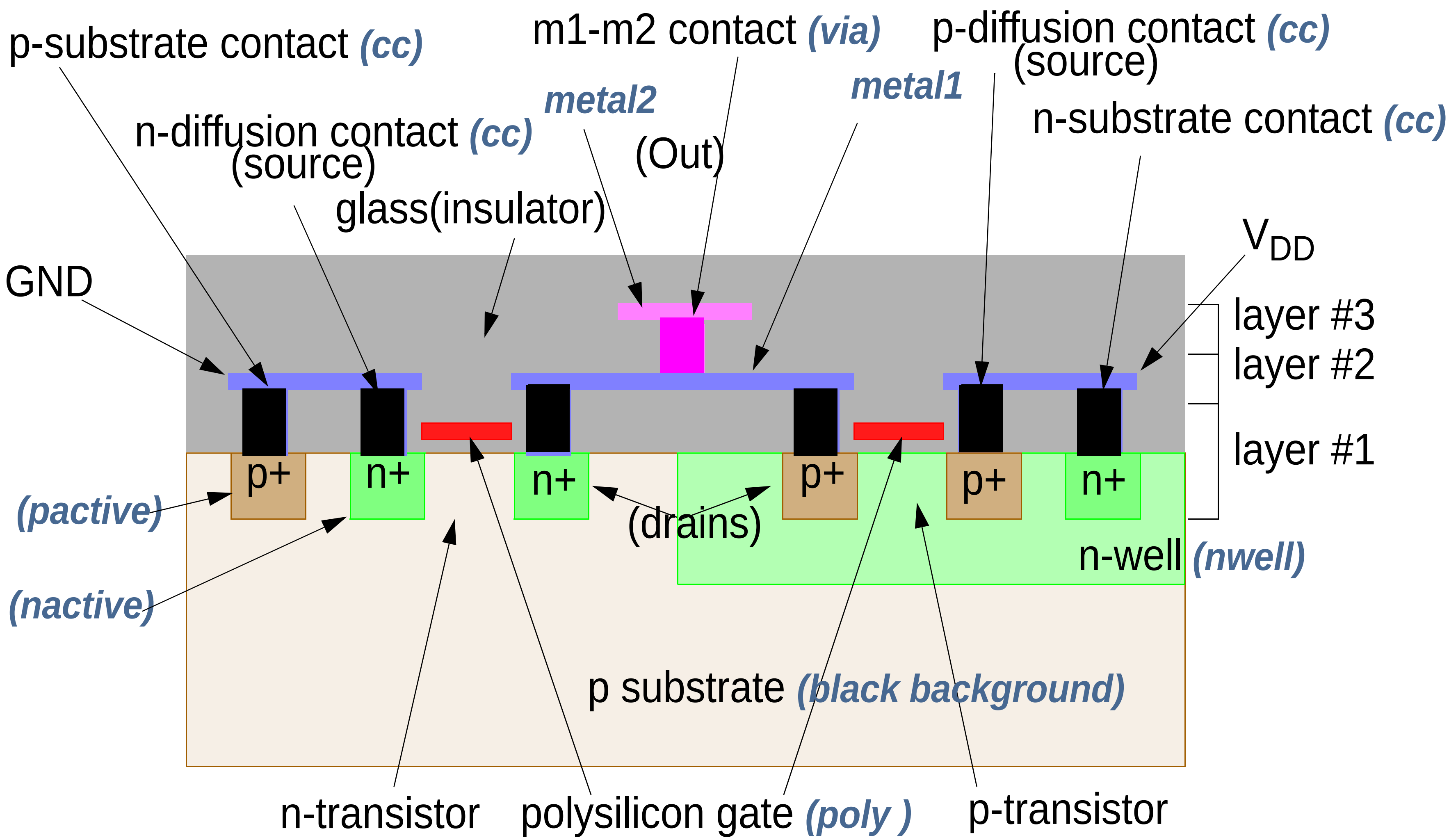
Four terminal devices: Source, Gate, Drain, body (substrate, bulk).





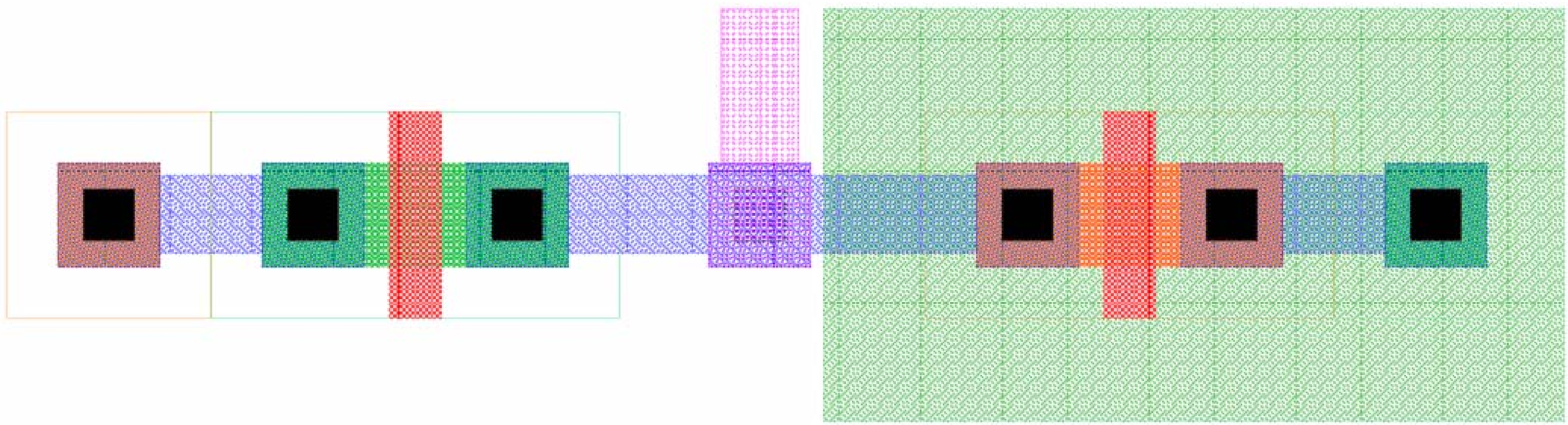
CMOS Inverter Cross-Section

Cadence Layer's for AMI 0.6mm technology



CMOS Cadence Layout

Cadence Layout for the inverter on previous slide

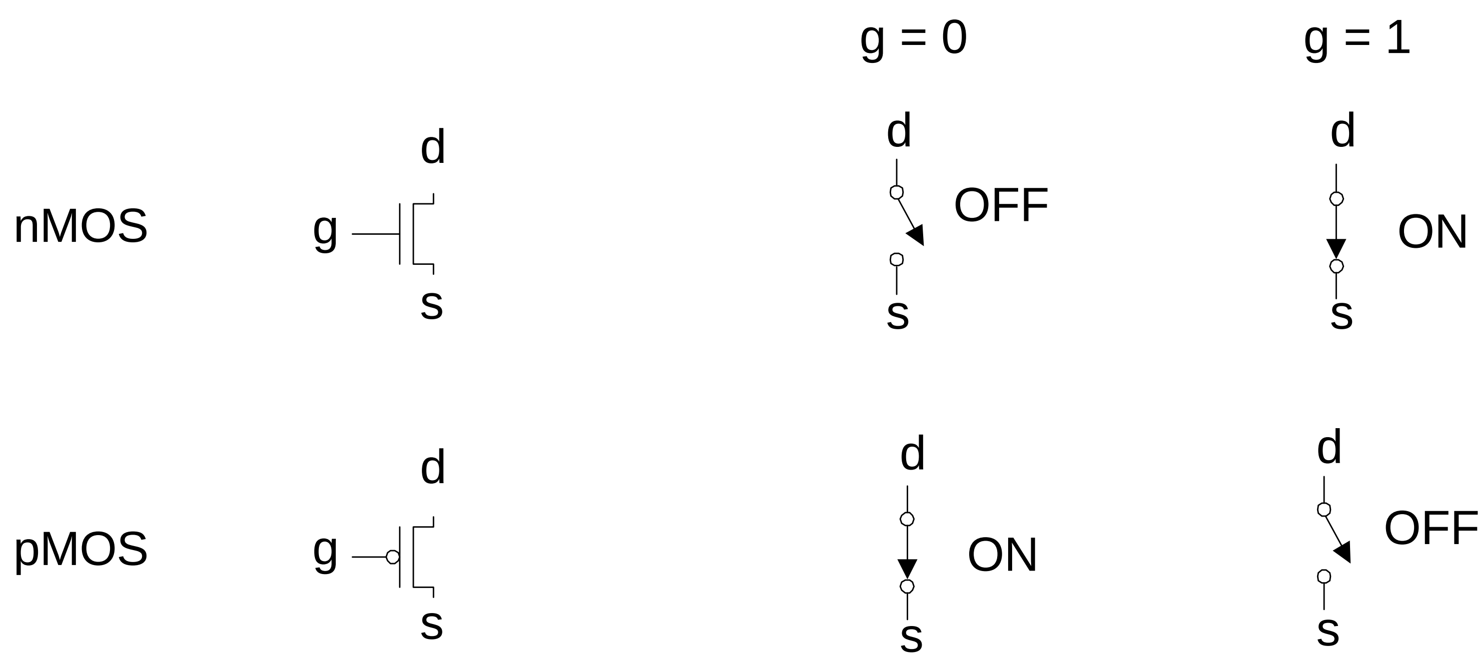


MOS Transistor Switches

We can treat MOS transistors as simple on-off switches with a source (S), gate (G) (controls the state of the switch) and drain (D).

1 represents high voltage, V_{DD} (5V, 3.3V, 1.8V, 1.2V, <=1.0V today, ...)

0 represent low voltage - GND or V_{SS}. (0V for digital circuits)



Signal Strengths

Signals such as *1* and *0* have strengths, measures ability to sink or source current

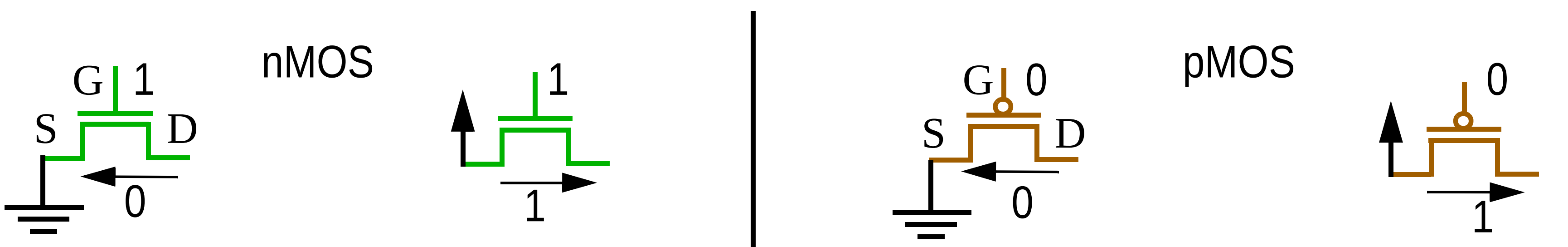
- V_{DD} and GND Rails are the strongest 1 and 0

Under the switch abstraction, G has complete control and S and D have no effect.

- In reality, the gate can turn the switch on only if a potential difference of at least V_t exists between the G and S.
- We will look at V_t in detail later on in the course.

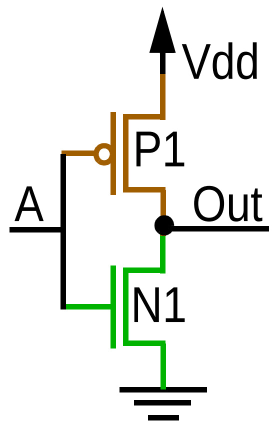
Thus signal strengths are related to Vt and therefore p and n transistors produce signals with different strengths

Strong 1: V_{DD}, *Strong 0:* GND, *Weak 1* :(~V_{DD} -V_t) and *Weak 0* :(~GND + V_t).

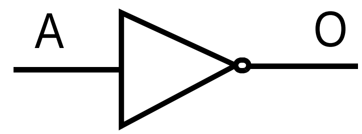


*** Strong 0*** Weak 1 Weak 0 *** Strong 1***

CMOS Inverter

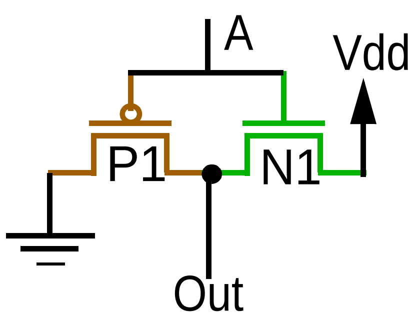


CMOS Inverter



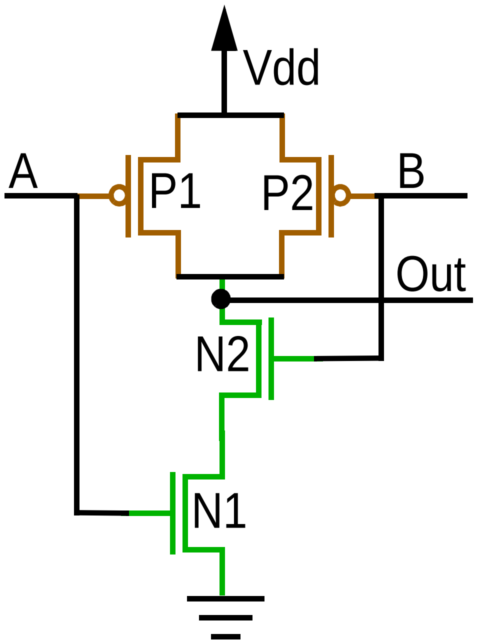
A	O
0	1
1	0

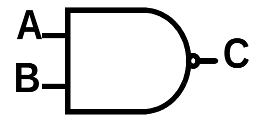
THE CONFIGURATION BELOW FOR A BUFFER IS NOT A GOOD IDEA. WHY?



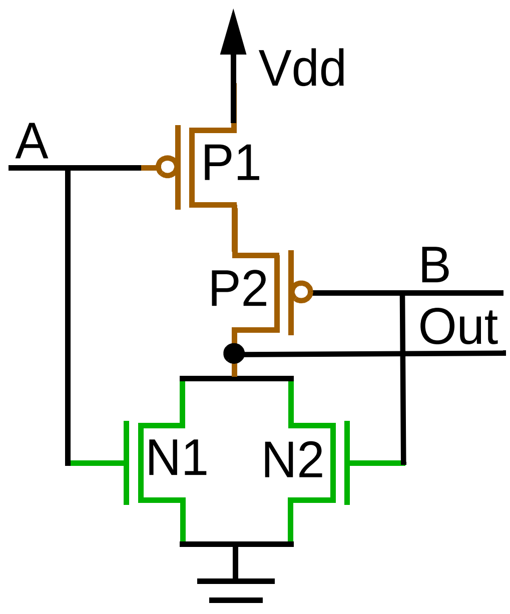
BAD IDEA

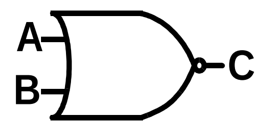
NAND and NOR CMOS Gates





A	B	C
0	0	1
0	1	1
1	0	1
1	1	0

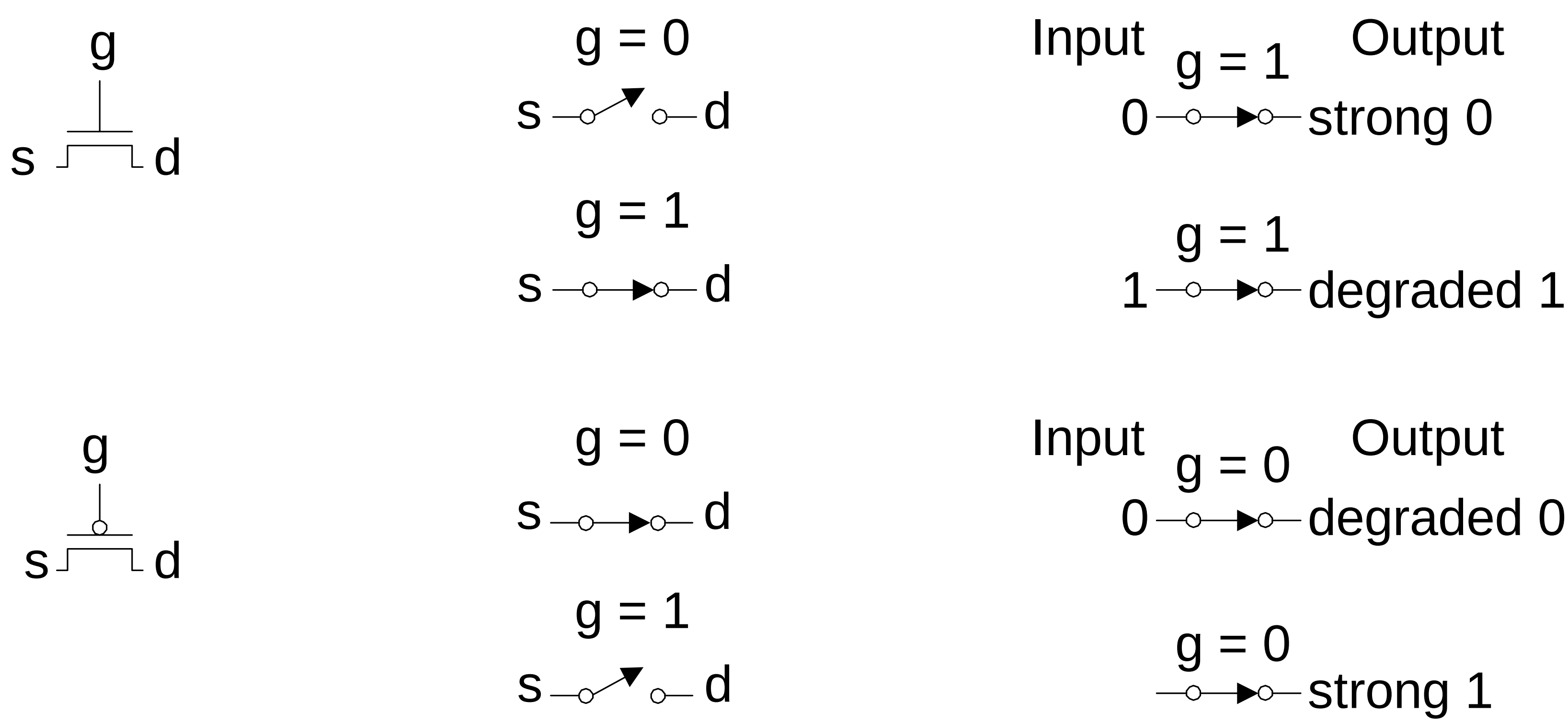




A	B	C
0	0	1
0	1	0
1	0	0
1	1	0

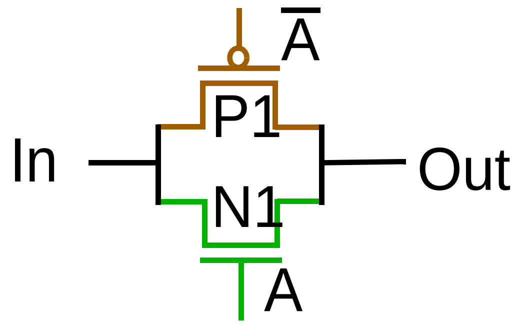
Pass Transistor

The off-state of a transistor creates a high impedance condition Z at the drain. No current flows from source to drain. So transistors can be used as switches.



However, as we previously discussed this will produce degraded outputs, if only one transistor is used as a switch.

Transmission Gates

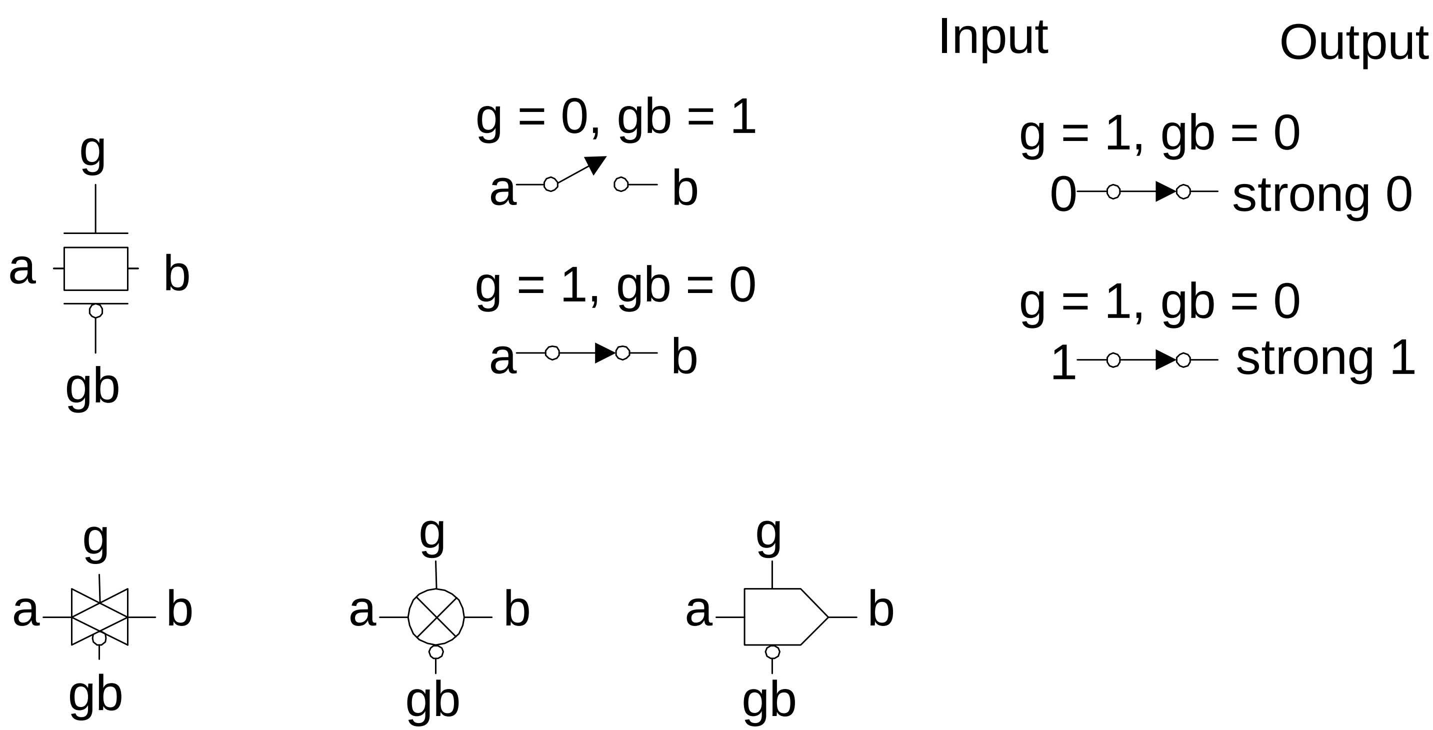


One pMOS and one nMOS in parallel.

Note that neither transistor is connected to V_{DD} or GND.

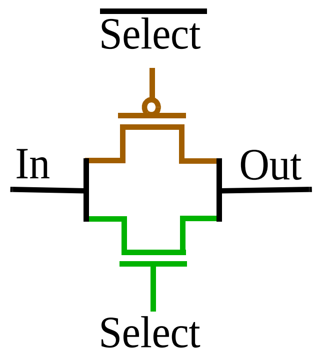
A and $\overline{A}$ control the transmission of a signal on *In* to *Out*.

Transmission gates act as tristate buffers.

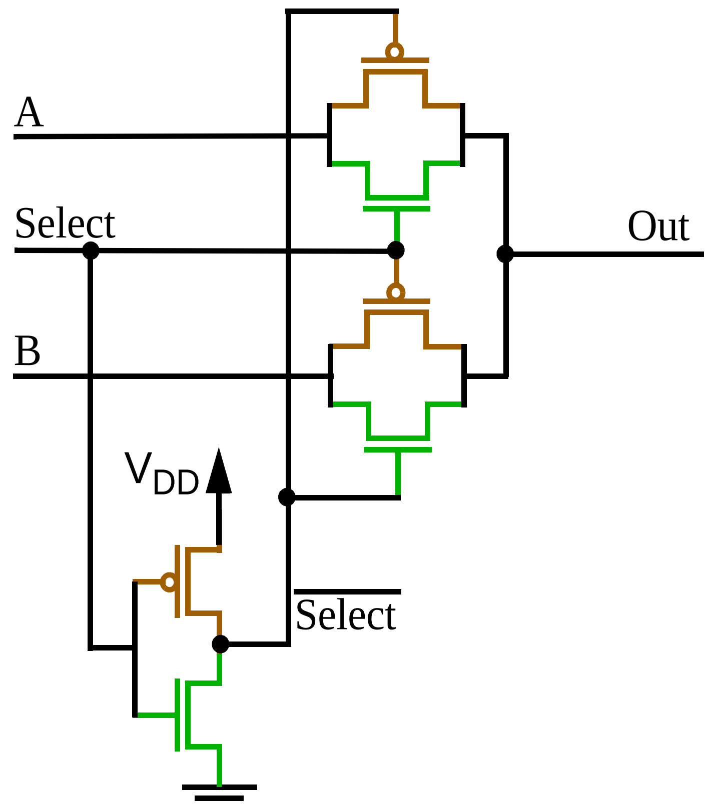


Transmission Gate Application: Select Mux

Transmission Gate



2-to-1 MUX



Truth Table for 2-to-1 MUX

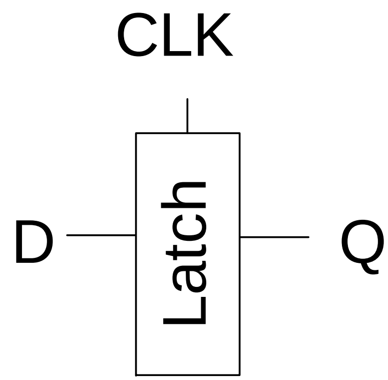
Select	Out
0	B
1	A

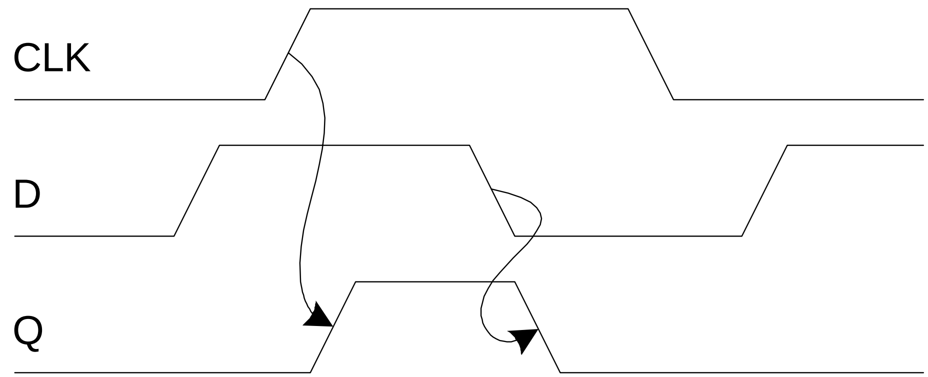
$\text{Out} = A.S + B.\overline{S}$

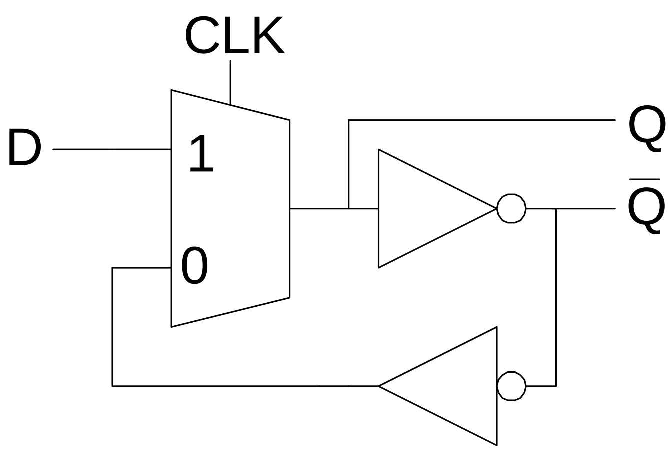
How many transistors are required to implement this using CMOS gates?

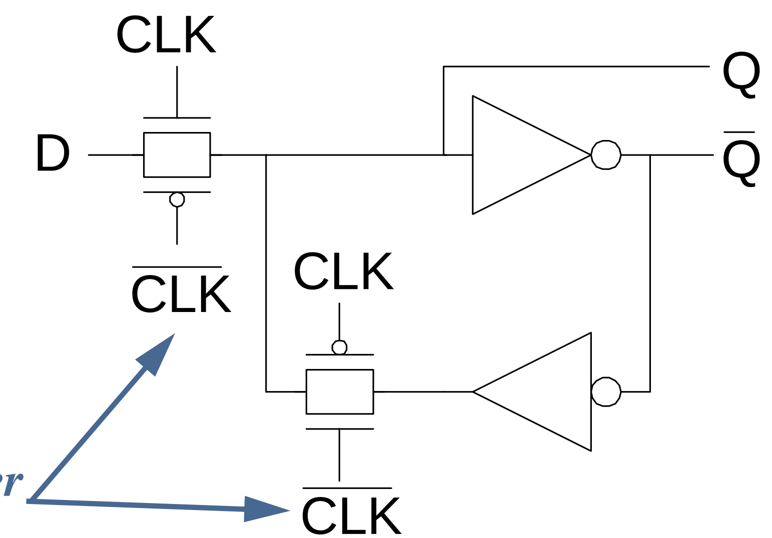
D Latch

Positive
level-sensitive
latch





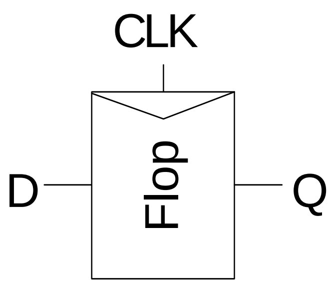


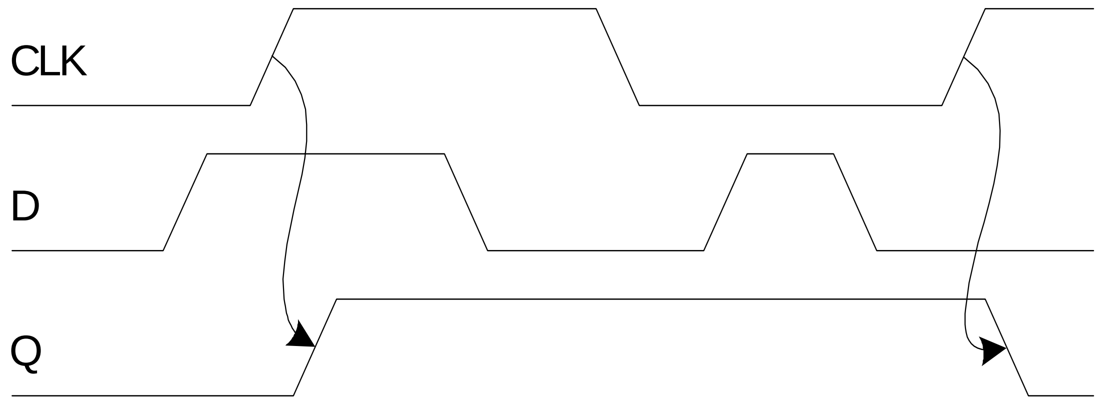


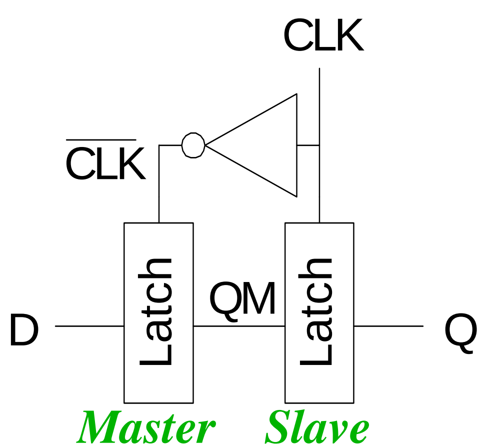
If $\overline{CLK}$ is unavailable one extra inverter needed to generate it using CLK

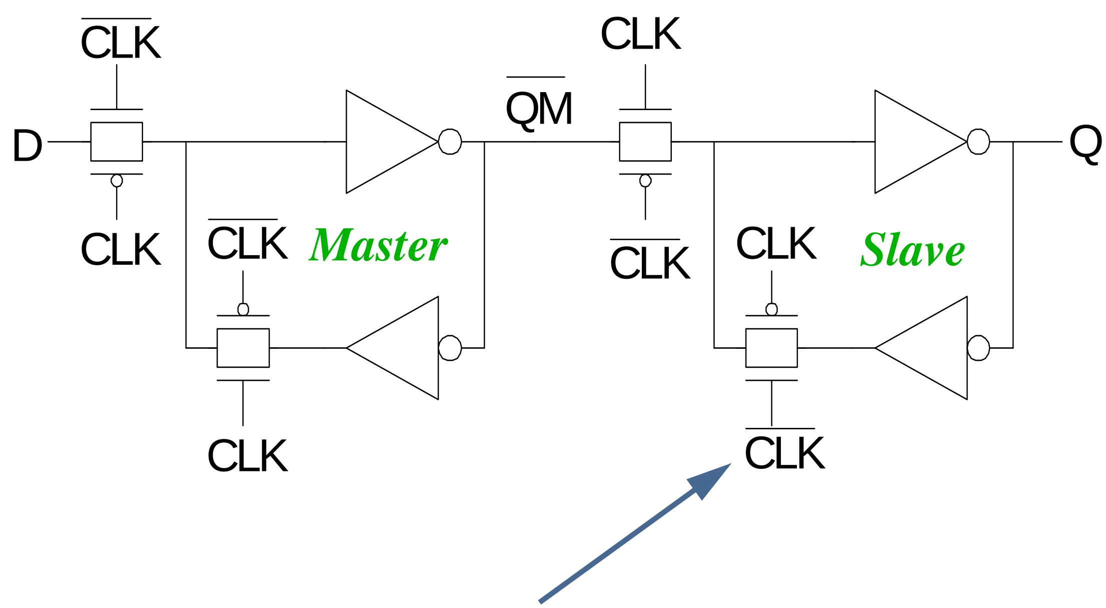
D Flip-Flop

Positive ***edge-triggered*** flip-flop a.k.a ***master-slave*** flip-flop







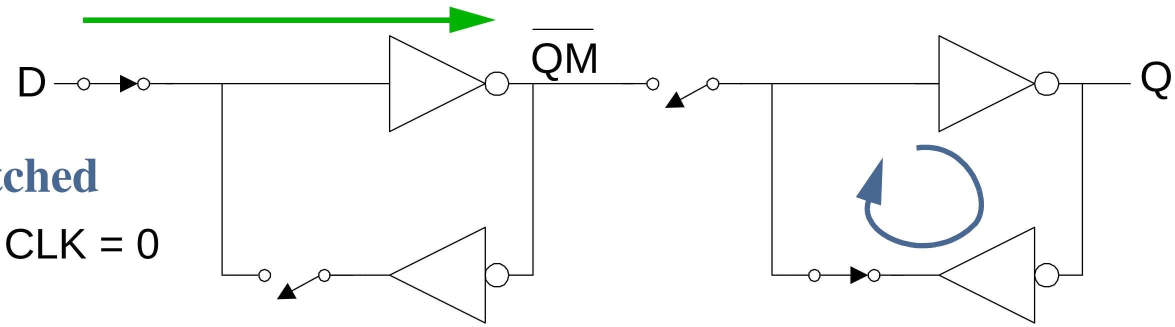


If $\overline{CLK}$ is unavailable one extra inverter needed to generate it using CLK

D Flip-Flop Operation

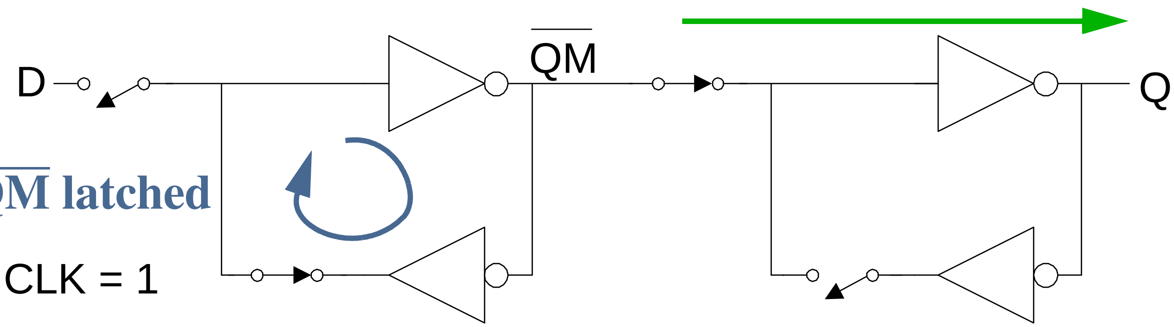
$\overline{QM}$ follows D, Q is latched

CLK = 0

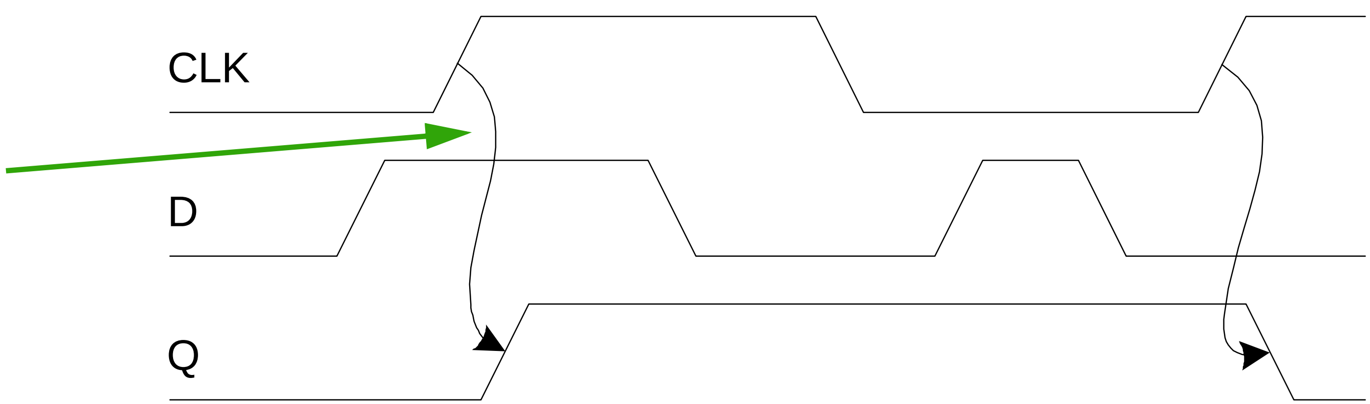


$\overline{QM}$ transferred to Q, $\overline{QM}$ latched

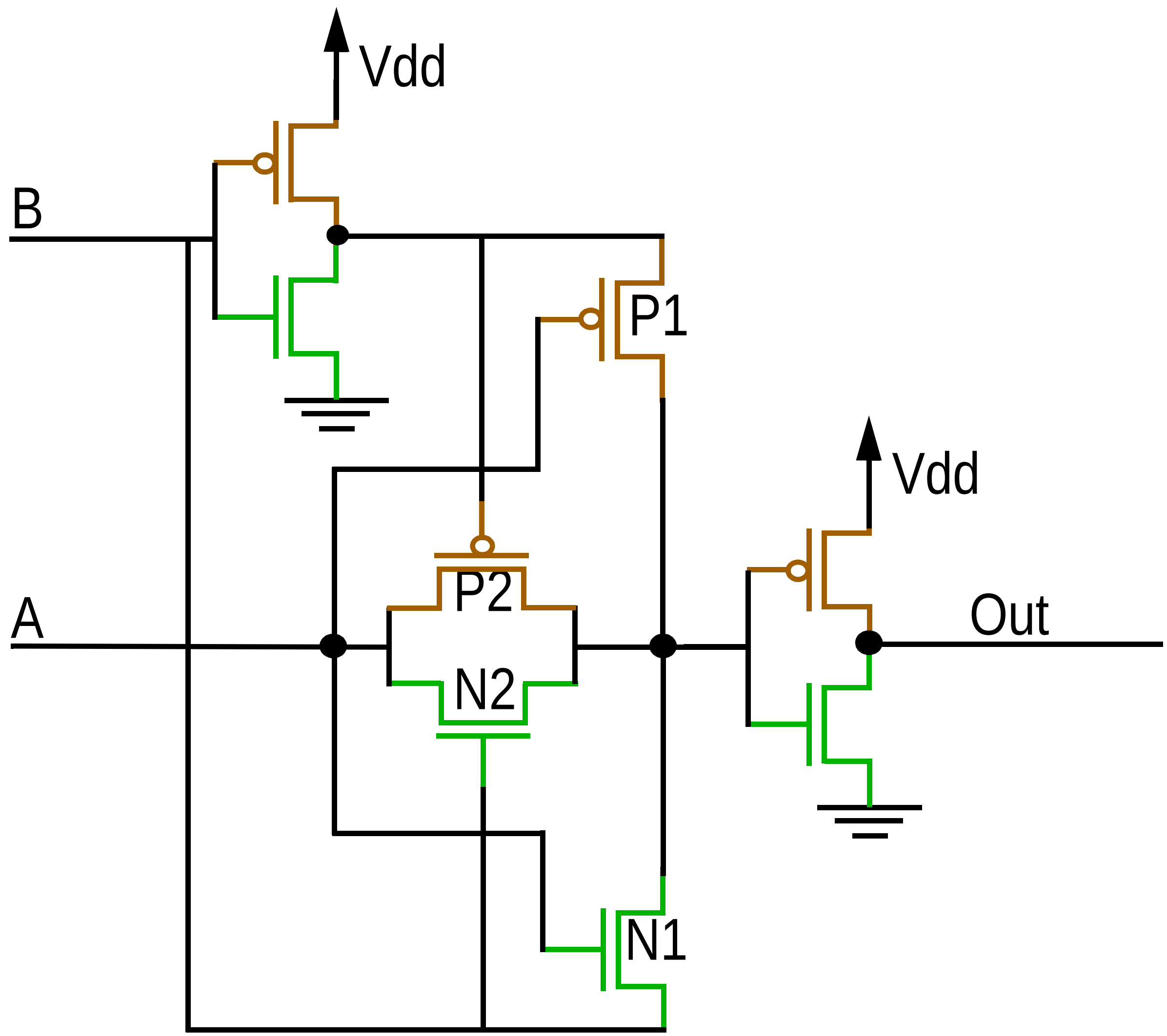
CLK = 1



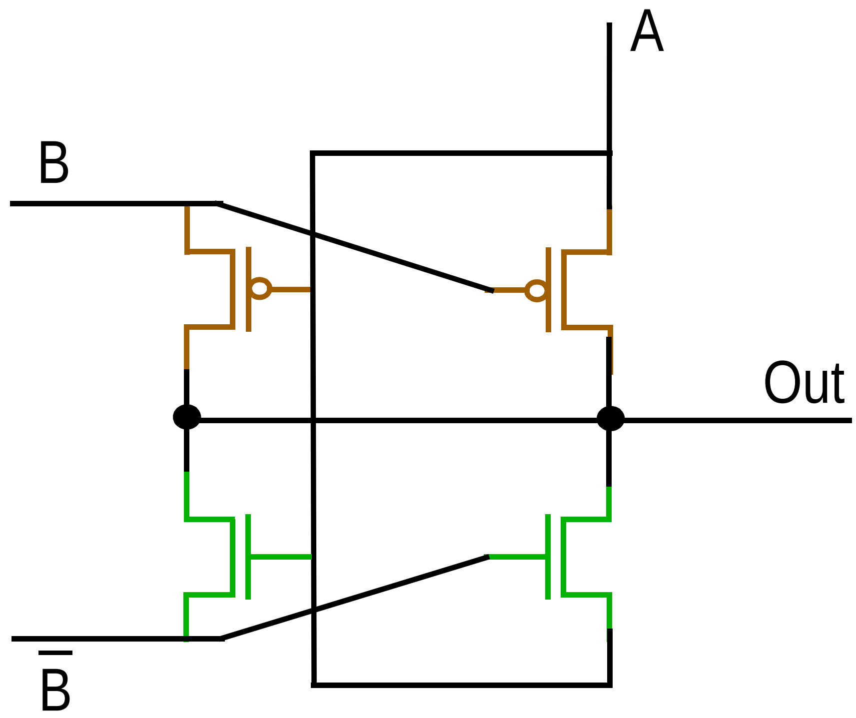
Positive
edge-triggered
flip-flop



More CMOS Gates



And More CMOS Gates



And More CMOS Gates