Simulation with Cadence Analog Design Environment

Analog Design Environment (ADE) is integrated on Cadence Custom IC Design software. You can simulate your design (schematic, extracted layout, vhdl, etc.) using the ADE.

This tutorial explains necessary steps required in preparing your design and using ADE to simulate the circuit. The tutorial assumes that you have the inverter cell with schematic and symbol views created as described in "Virtuoso Schematic Composer Tutorial" (available on class website).

Simulation Cell View Preparation

The first step is to prepare the simulation schematic view. In this tutorial, we will simulate the inverter using pulse voltage source connected at its input. First, create new schematic view by go to File -> **New -> Cell View**, we will call this cell **inverter_sim** as shown in Figure 1.

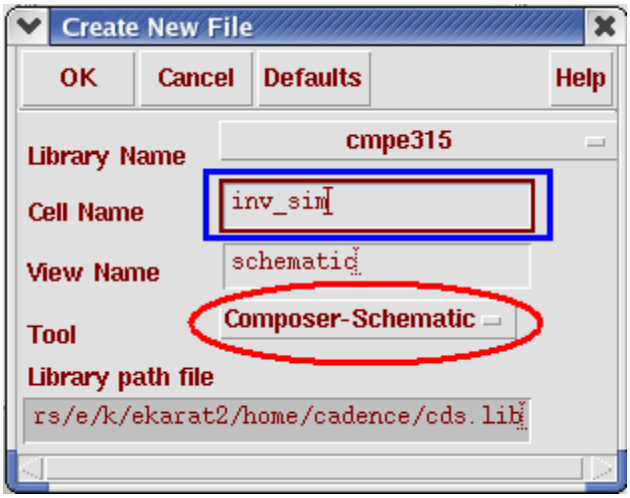

Figure 1: New simulation cell view

Next, we need to place the symbol of inverter on the schematic. Create new instance of the inverter by select "inv" from "cmpe315" library from the component browser as shown in Figure 2. At the Add Instance dialog, make sure you have **symbol** selected as shown in Figure 3, if not you can manually type in or click Browse.

Create instances of vdd, gnd, vdc and vpulse, create new OUTPUT pin (with "output" direction) and then make appropriate connections as shown in Figure 4. You can find vdc and vpulse from **Voltage_Sources -> vdc**, **Voltage_Sources -> vpulse** in **NCSU_Analog_Parts** library.

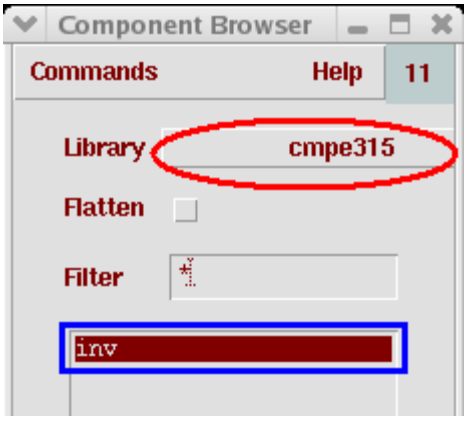

Figure 2: Select inv (inverter) cell from Component Browser

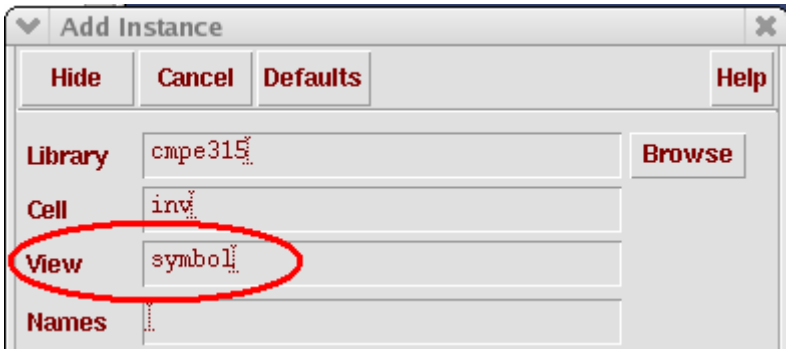

Figure 3: Select symbol view of inv cell

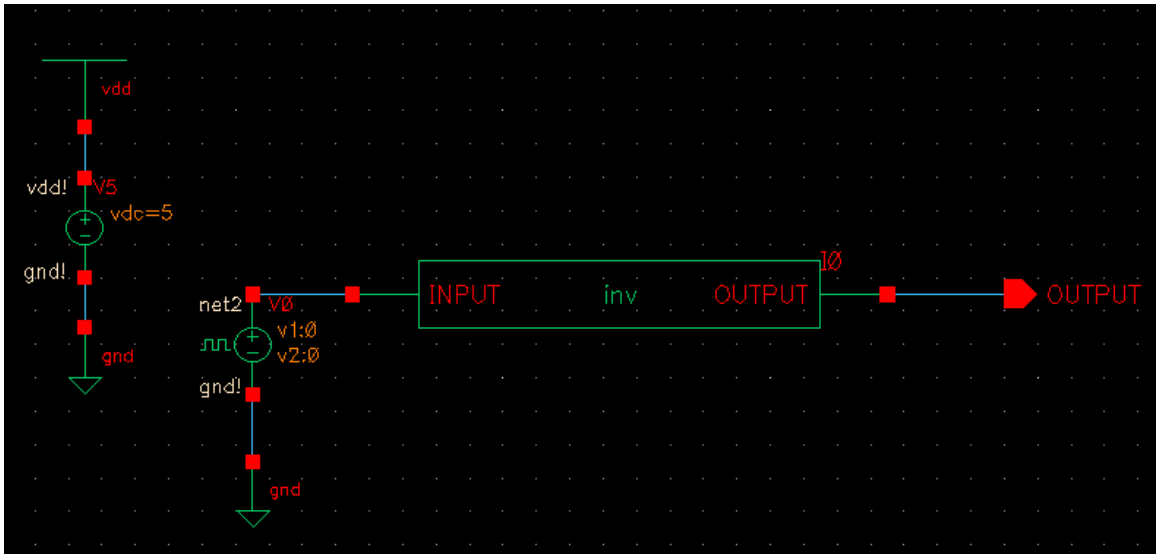

Figure 4: Schematic of inv_sim

Now, we need to change the properties of vdc and vpulse. To change the property, click on the component and go to **Edit -> Properties -> Objects**. For vdc, set DC voltage to 5V as shown in Figure 5. For vpulse, set Voltage1 to 0V, Voltage2 to 5V, Delay time to 1ns, rise and fall times to 500ps, pulse width to 5ns and period to 10.1ns as shown in Figure 6.

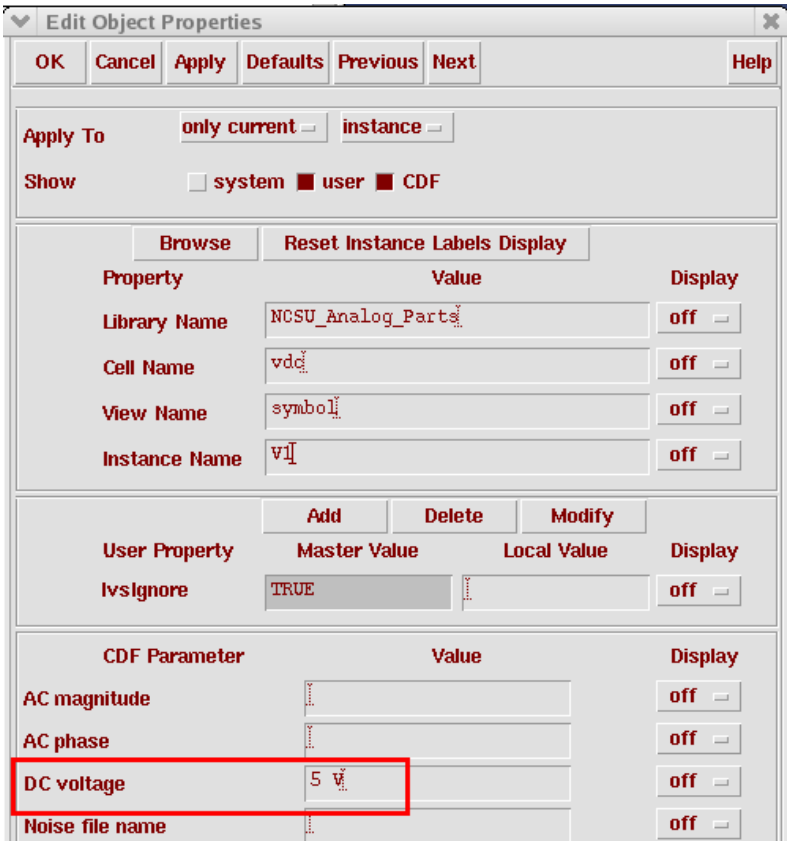

Figure 5: Property of vdc used for the simulation

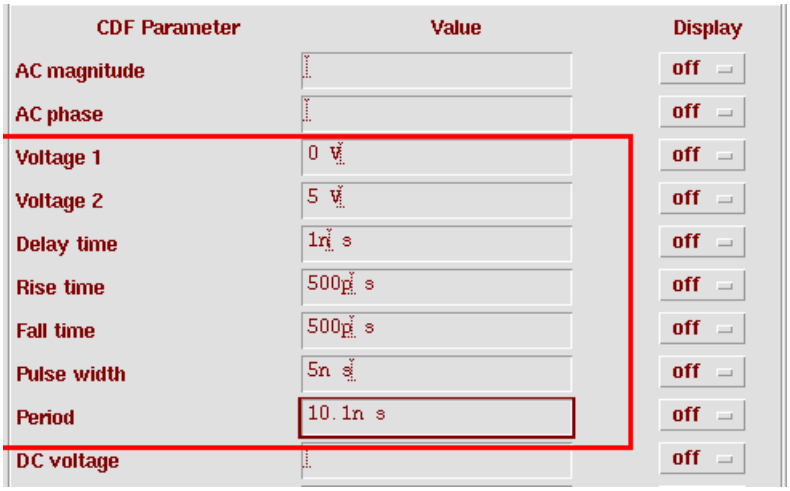

Figure 6: Property of vpulse used for the simulation

Hierarchy Editor

Hierarchy Editor lets you change views of the cell for simulation. For example, if you have made the schematic and layout for the inverter, you can create only one simulation view and then switch between schematic or extracted layout in the simulation using Hierarchy Editor. You can also mix multiple view types of cells in simulation using Hierarchy Editor (This mean you can simulate schematic of adder connects to layout of multiplier and/or vhdl of control logic).

To create new Hierarchy Editor view, highlight inv_sim cell in Library Manager, go to **File -> New -> Cell View** and select **Hierarchy-Editor** tool as shown in Figure 7.

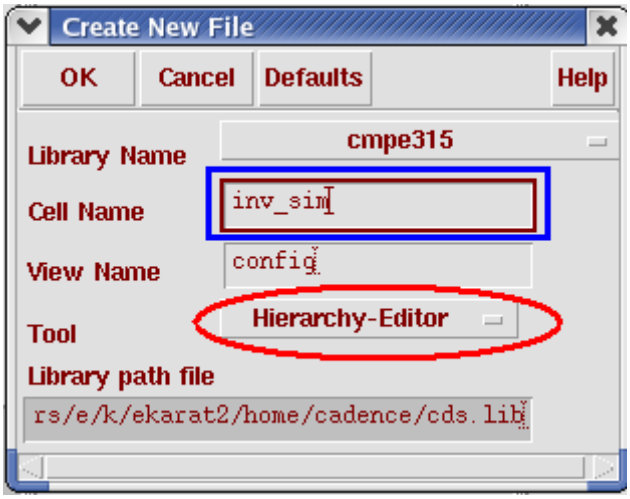

Figure 7: New Hierarchy Editor view

The New Configuration dialog will show up, click **Browse** and select schematic of inv_sim as the top cell as shown in Figure 8. Then click **Use Template**, another dialog will appear as shown in Figure 9, select **spectreS** template and click OK. At View List, add "**extracted structural schematic**" separated by spaces exactly as shown in Figure 10. Click OK to close New Configuration dialog.

Now you will see Hierarchy Editor dialog as shown in Figure 11. From here, you can specify view you want to use in the simulation. For us, we will use schematic view of inverter in the simulation, so type in **schematic** in **View to Use** column of **inv** cell as shown in the figure. Click  icon to save the configuration and then close the Hierarchy Editor.

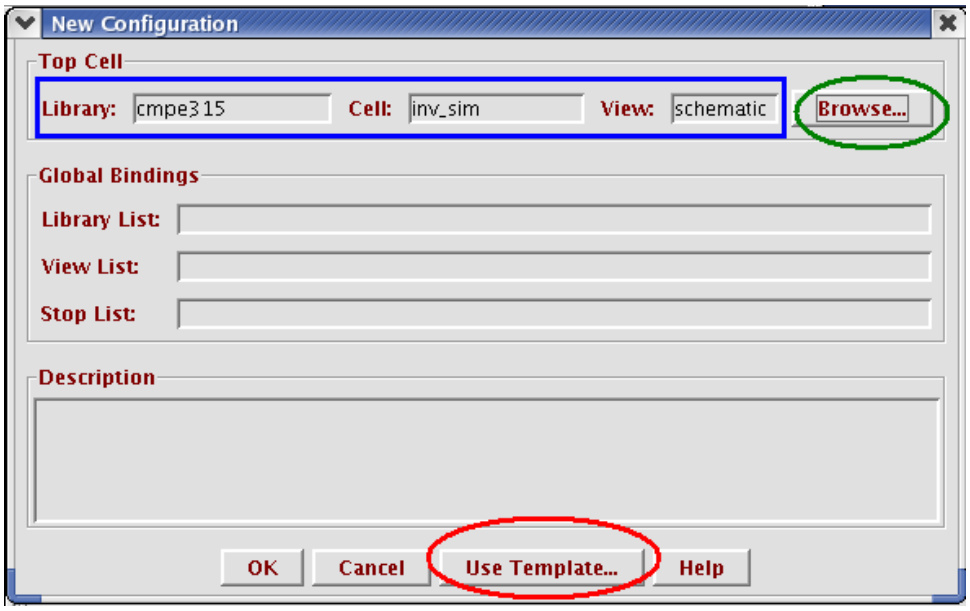

Figure 8: New Configuration

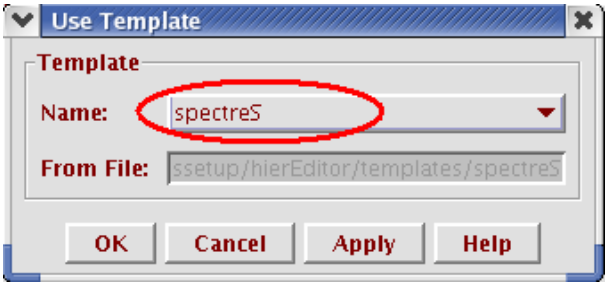

Figure 9: Use Template

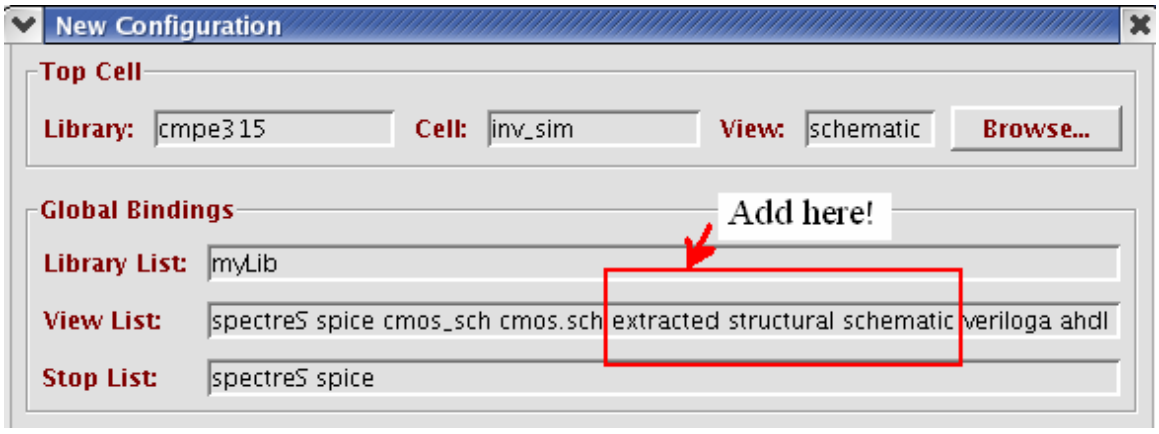

Figure 10: Add "extracted structural schematic" to View List

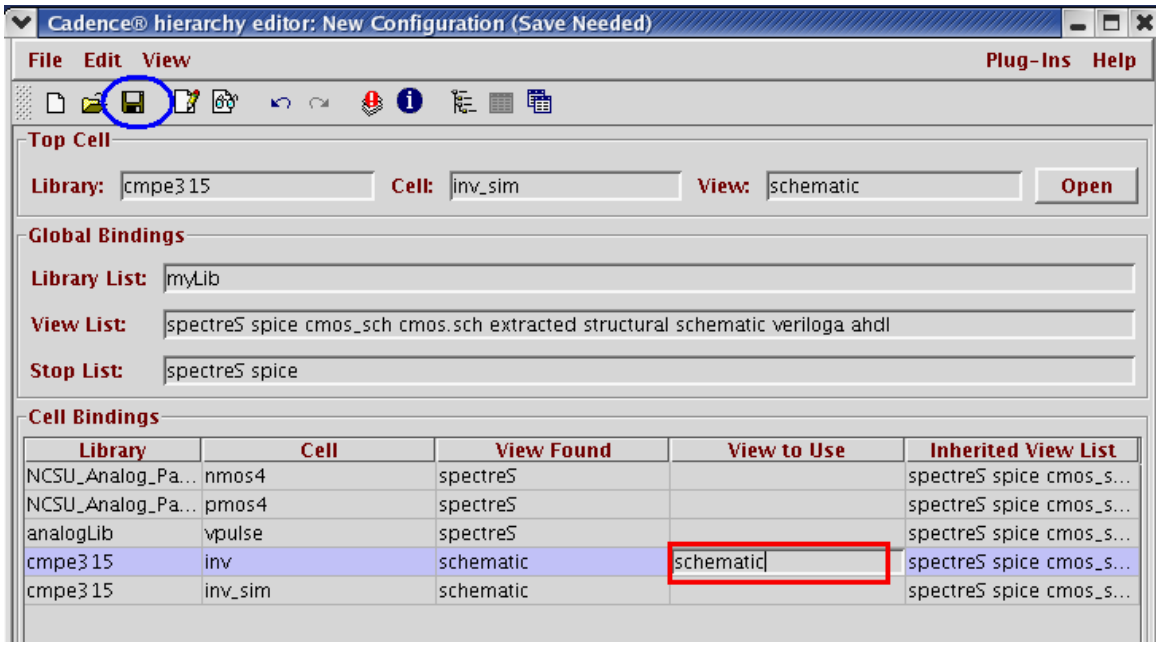

Figure 11: Hierarchy Editor

Open Analog Design Environment (ADE)

Open the config view of inv_sim cell (by double clicking), the dialog as shown in Figure 12 will show up, click OK. The schematic of inv_sim should be opened, go to **Tools -> Analog Environment**. The ADE window should appear as shown in Figure 13.

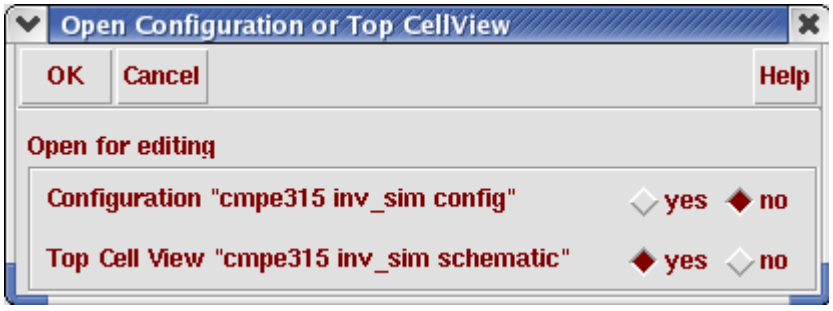

Figure 12: Open config view

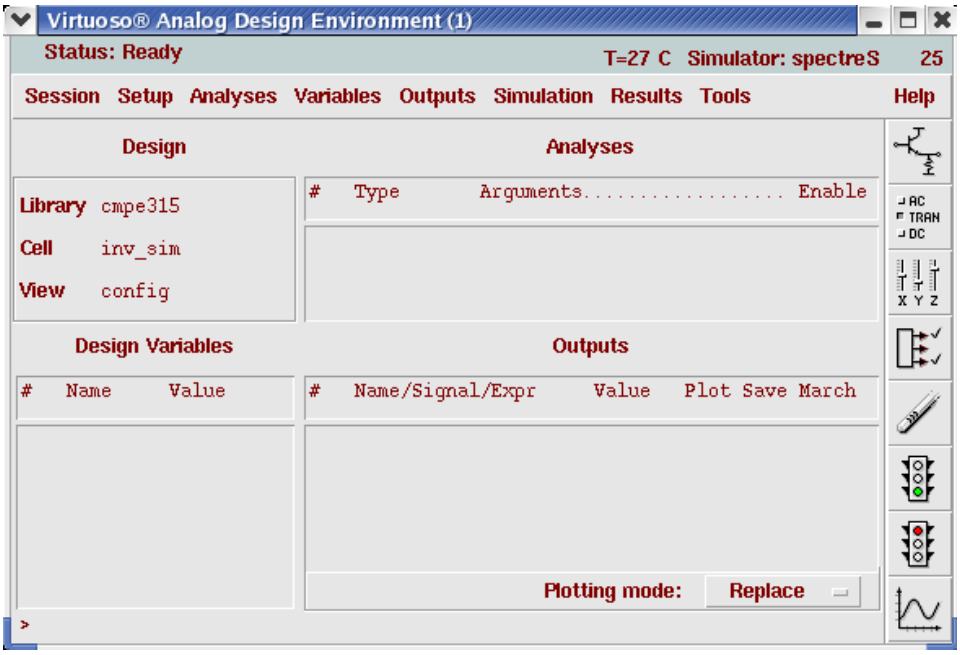

Figure13: Analog Design Environment

Simulation Setup

Next, we need to set the type of analysis, stop time and accuracy level for the simulation. Go to **Analyses -> Choose**, the Choosing Analyses dialog will appear. Select **tran** for analysis type, enter **25n** (run simulation for 25ns) for stop time, click on **conservative** for accuracy mode and **Enabled** to enable this simulation setup as shown in Figure 14.

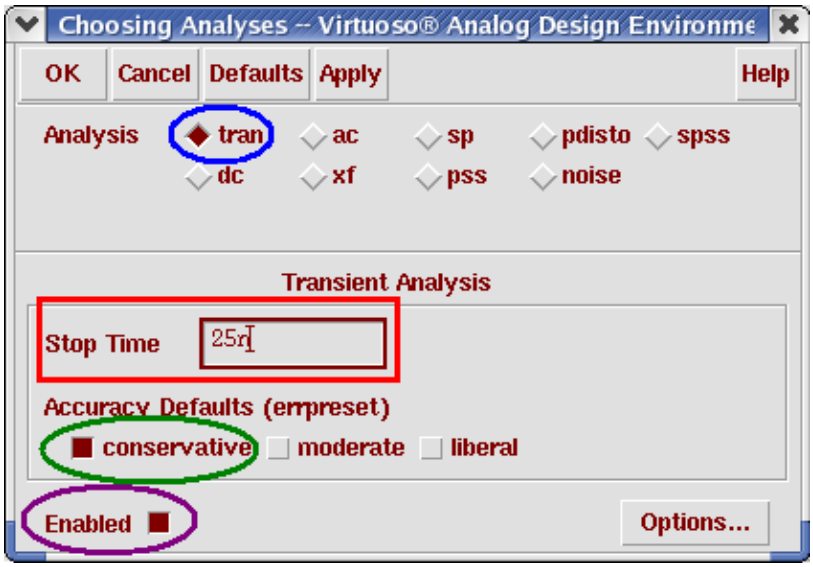

Figure 14: Choosing Analyses

Next, we will select signals we want to observe after run simulation. Go to **Outputs -> To Be Plotted -> Select On Schematic**. Click on wires/nets on schematic that you want to observe. In our case, click wire connected to INPUT and OUTPUT of the inverter. The ADE window after having analyses and outputs setup is shown in Figure 15.

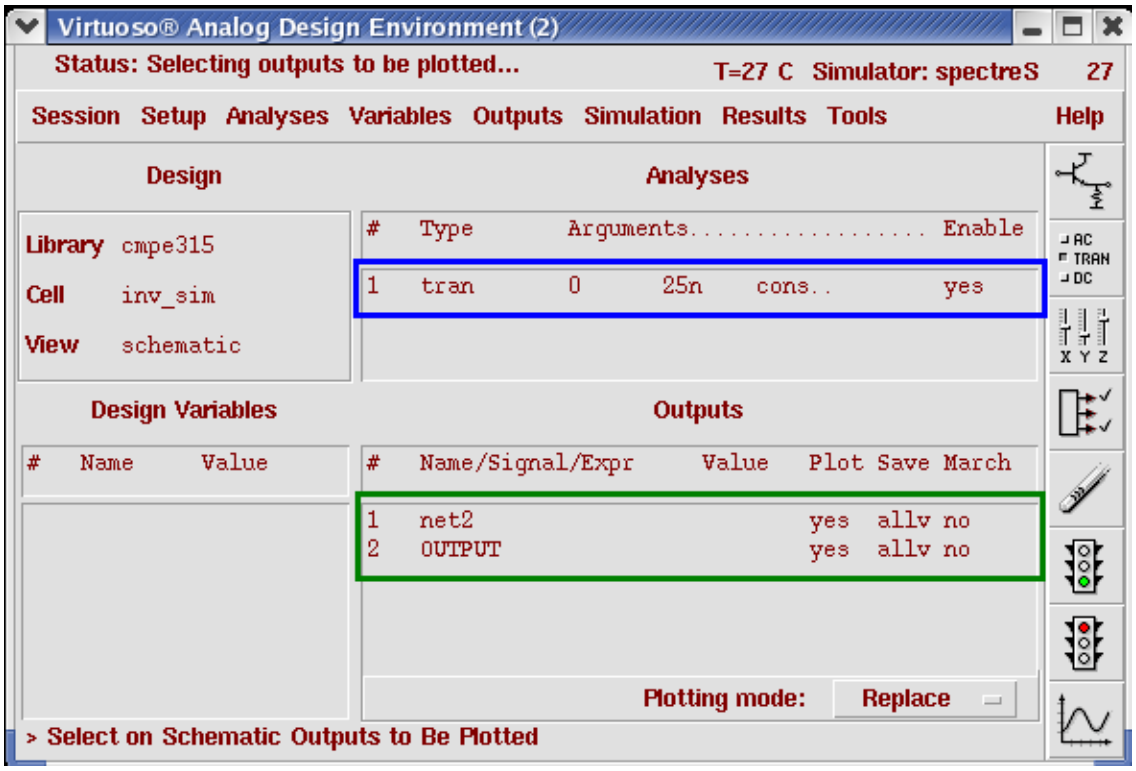

Figure 15: ADE after analyses and outputs setup

Go to **Simulation -> Create Final**, the final netlist will appear as shown in Figure 16. If the netlist does not show up, see if there are any errors on CIW window or go to **Simulation -> Output Log**. (Note that this step may be skipped but we recommend you to run if you are setting the new simulation for the new cell.)

More info:

- SpectreS is a simulator used in this tutorial and it is selected for you by default. We have the correct simulation models required for SpectreS setup in ADE for you. However, ADE can run many other simulators including cdsSpice, Spectre, UltraSim, etc.
- UltraSim is a fast Spice simulator. The UltraSim provides many useful options to trade off between simulation speeds and accuracy. You might want to use UltraSim to simulate large circuit especially large parasitics extracted layout.

Figure 16: Created Final Netlist

Run Simulation

Now run the simulation, go to Simulation -> Run. If the circuit is large, it might take times for the simulation to finish (depends on the size of the circuit, might take from few minutes to many hours). The information on running simulation is displayed on CIW window.

Simulation Results on Waveform Window

After the simulation is finished, the waveform window will show up as shown in Figure 17. All signals selected will plotted on the same axes and difficult to look at some time. Go to **Axes -> To Strip** to have waveforms plotted on separate axes as shown in Figure 18.

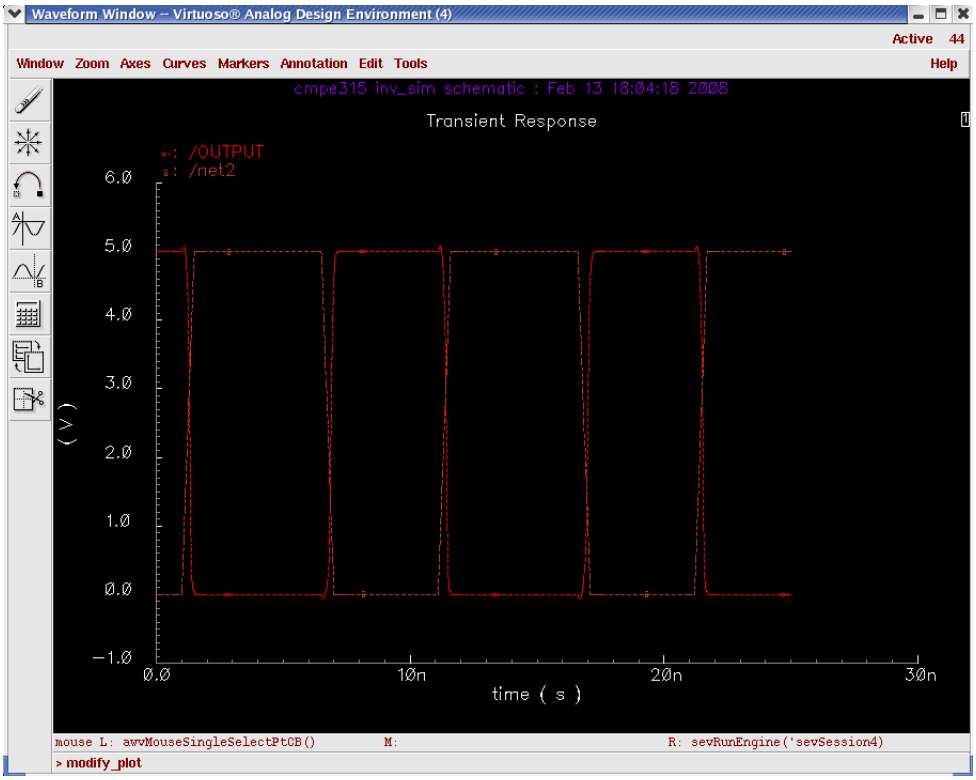

Figure 17: Waveform Window

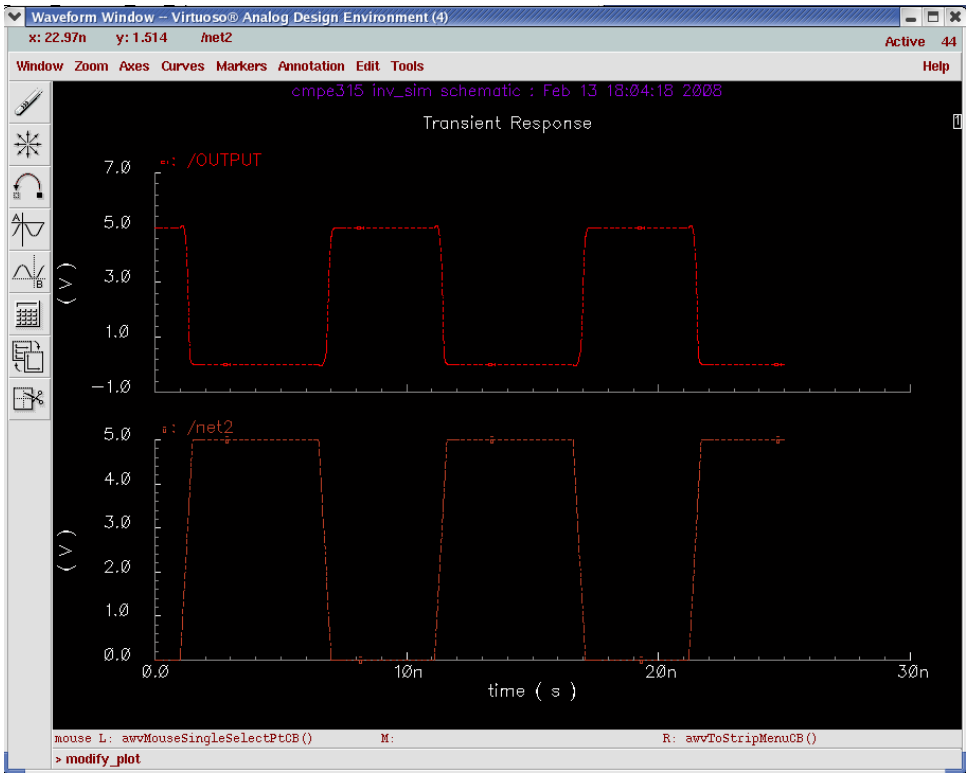

Figure 18: Waveform Window after Strip

Waveform Hardcopy

To save waveforms displayed on Waveform Window, go to **Window -> Hardcopy**. Enter file name you want to be saved (postscript file).

Save State

You can save simulation setting so that next time you open ADE you do not need to setup Analyses and Output to be plotted (and any other settings) again. Go to **Session -> Save State**, enter state name as shown in Figure 19 and then click OK.

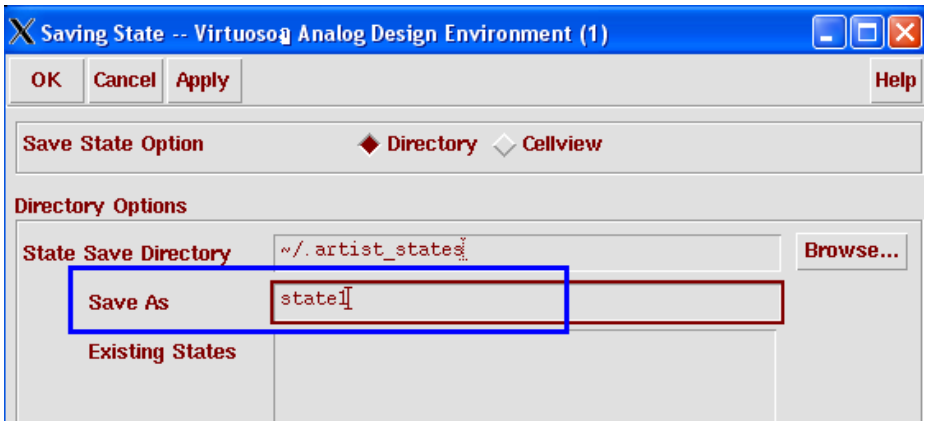

Figure 19: Save State

Load State

To load saved state, go to **Session -> Load State**, select the state you want to load from the list as shown in Figure 20.

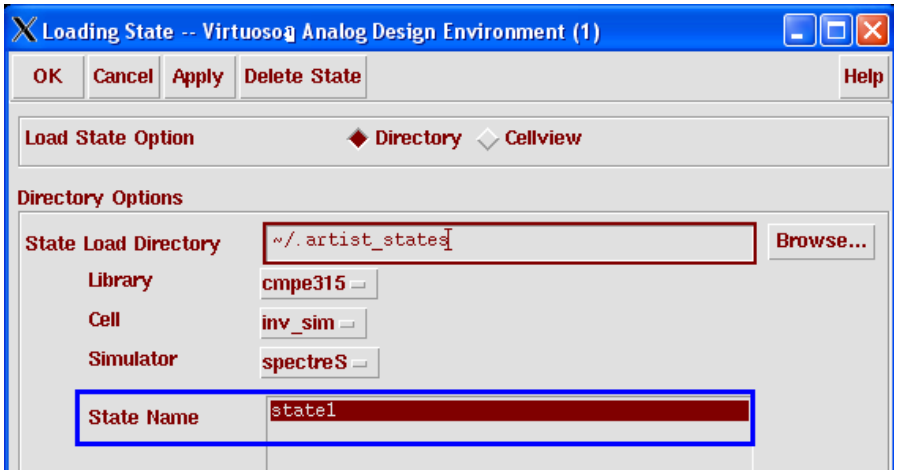

Figure 20: Load State