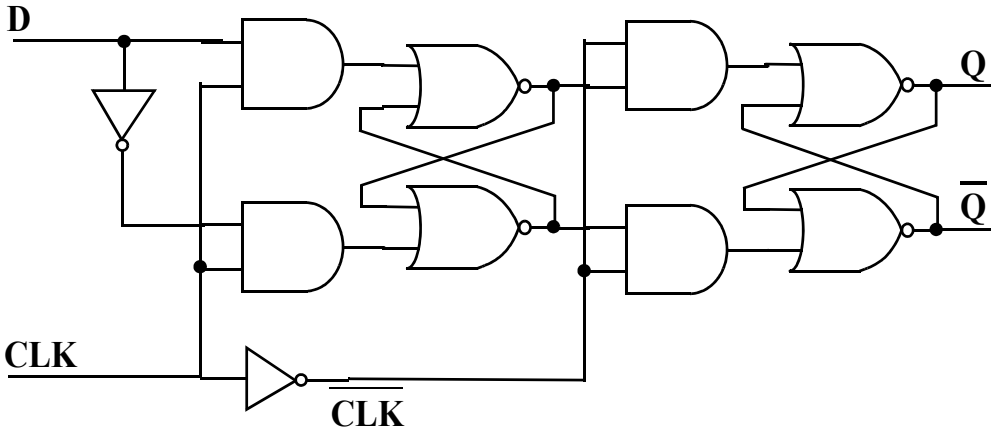
**CMPE 315 Lab**

## LAB Assignment #4 for CMPE 315 (200 points)

Assigned: Thrs, Sep 30th
Due: Thrs, Oct 14th

## Description: Layout and simulate both a transmission-gate master-slave flip-flop and a gate-level version:

- The layouts needs to be designed using the standard cell layout style discussed in class. The cell height should be 22.05 μm (measured from the nselect at the top and the pselect at the bot-tom, the nwell can extend over) with a Vdd rail at the top and Gnd rail at the bottom with widths of 1.8μm. You can make each cell of variable width. Use the n and p transistor ratio from your previous labs for all transistors. Use minimum size transistors for your transmission gates.
- Draw the schematic and layout the transmission gate flip-flop (negative edge triggered) discussed in class (***Basics*** slide set) as a single cell. You are allowed to use only poly and metal1 for routing.
- Draw the layouts for the individual gates below using the above constraints. You are allowed to use only poly and metal1 for routing in each of these cells. Draw the schematic and layout of the gate-level version shown below using instances of the cells you already created. You can use metal2 and metal3 to make connections between instances.:




## Report Requirements:

(1) Print out the schematics and layouts.

(2) Run simulations on both schematics and extracted views showing the functionality. Generate plots to show that both flip-flops are functionally correct. i.e. they can latch a one and a zero properly.

(3) For both flops, run simulations on the extracted view to determine the setup time (and hold time as well for CMPE 640 only) for the flip-flop when latching a zero and a one. We will discuss the simulations that you need to perform during the discussion session. For all simulations use

100ps as rise and fall times for both D and CLK. The output should be driving 4 INVx1 inverter schematics.
(4) Include waveforms that show the flip-flop failing to latch the correct data for both cases (from the parametric sweeps). There should be waveforms for the coarse grained sweep as well as the fine grained sweep.

(5) Generate the following plots and determine the times values given below for both cases. Report all the data in a table.

- Plot the clk-to-q ($t_{cq}$) delay (y-axis) versus the d-to-clk ($t_{dc}$) delay (x-axis). Determine the following time values:
  1. Min Delay: minimum $t_{cq}$ value (i.e. $t_{cq}$ when d changes a "long time" before clk)
  2. Failing Delay: $t_{dc}$ when the flip-flop fails to latch the correct value
  3. Setup Time 1: $t_{dc}$ when the $t_{cq}$ increases by 10% over the minimum value
- Plot the total d-to-q ($t_{dq}$) delay (y-axis) versus the d-to-clk ($t_{dc}$) delay (x-axis). Determine the following time value:
  1. Setup Time 2: $t_{dc}$ when the $t_{dq}$ is minimum
- You need to generate the plots and determine the time values for both cases i.e. the flip-flop latching a 1 as well as latching a 0
- CMPE 640: You need to generate the same plots for hold time and calculate similar values

(6) Use the guidelines outlined in Lab 2 for the report. All the plots should be labelled, captioned and referred to in your write-up. The write-up should be brief and contain the simulation parameters used for each experiment and describe the corresponding plots.

(7) Submit a single pdf file for your report using submit, the class name is cmpe315_cpatel2 and the project name is lab4.

**THE LABS ARE INDIVIDUAL EFFORTS: INSTANCES OF CHEATING WILL RESULT IN YOU FAILING THE COURSE.**