LAB Assignment #2 for CMPE 315 (200 points)

Assigned: Thrs, Sep 16th
Due: Mon, Sep 27th

Description: Schematic Design and SpectreS Simulations

1. Design a minimum sized inverter (INVx1) schematic using the AMI 0.6um technology. Design a simulation view using schematic and hierarchy editor. In the simulation view the inverter should be driving four copies of itself. Run simulations using Spectre and size the PMOS transistor in the inverter schematic to obtain roughly equal output rise and fall times (<= 5% difference). The input source should use 100ps rise and fall times for this simulation.
2. Design simulation views and run simulations using the above inverter driving 1, 2, 4, 8 and 16 copies of itself. Measure the rising and falling transition delays as well as the rise and fall times for each case. Input source rise/fall times should be 100ps.
3. Design inverters with x2 (INVx2) and x4 (INVx4) drive strengths by sizing both the NMOS and PMOS transistors. Repeat step 2 for each of these inverters using the INVx1 as the load inverter(s).
4. Design a 2-input NAND (NAND2x1) gate and a 2-input NOR(NOR2x1) gate. We will discuss the transistor sizes required during lab discussion. Perform simulations with 1,2 and 4 INVx1 as the load inverter(s). For these simulations hold one input constant and switch the other input to obtain an output transition. Perform simulations for (input 1 constant, input 2 switching) as well as (input 1 switching, input 2 constant). Report the differences, if any, for the two cases.

Report Requirements:

1) Briefly describe the steps required to create schematics, simulation views, running simulations and plotting results.
2) Provide schematic views for each of the gates above and at least one simulation view for each. Create a table with PMOS and NMOS transistor sizes for each of the gates that you have designed.
3) Provide plots with output waveforms for each of the cases that you have run simulations on. You can plot the outputs for each gate on a single plot.
4) Compute the rise and fall times for each simulation (measured at 10-90% points) as well as the delays (measured at the 50% points).
5) Summarize these computation using graphs. You are free to pick the format that you want to represent this data. Make sure all the data is being presented. The graphs should be such that you are able to explain to somebody else what simulations were performed, what parameters were used and what trends do you see in the results.
6) Provide observations about the output delay, output rise and fall times, with respect to drive strengths and output load.
7) Grading will be based on the completeness of your write-up and submission of the required plots. All the plots should be captioned and should be referred to in the write up. Mark each axes with proper signal names and format the names of the signal at the top of the plot. A significant portion of your grade will be based on the presentation and content of this lab report. Make sure

you index the report and number/caption all the figures and tables. You will be submitting a single pdf file for this report. The first page of the report should be the lab submission page. The class name to use for submit is cmpe315_cpatel2 and the project name is lab2.

THE LABS ARE INDIVIDUAL EFFORTS. INSTANCES OF CHEATING WILL RESULT IN YOU FAILING THE COURSE.