Project Submission I

VHDL Code

1. Write the VHDL code for the whole project. Make sure that you use a hierarchical design.
2. Simulate individual components and each level of hierarchy. Simulate the whole design when done. Also make sure you run exhaustive simulations on your design at the component level i.e. all possible patterns for the various building blocks should be used for the simulations.
3. Submit sample input & output files. Don't submit all possible combinations. Just a page of inputs and the corresponding outputs. Clearly mention the inputs and the outputs for each stage. Also submit the corresponding plots using the VHDL waveform GUI. You do not have to submit plots/results for the low level primitive cells. Plots for all the major components should be clearly marked with signal names and function performed.
4. Include an enscripted version of all your code and test benches. Test benches for low level primitive cells is not required. Thus if you use a cache cell to make up your cache there should be a file for the cache cell and then for the final cache. Clearly label each file. Simulations results for that particular design (mentioned above in 3) should immediately follow the code.
5. Write a description for the whole submission. It should mention design strategy that you used. A block diagram of the hierarchical breakup of you designs. (The block diagram that I have in the description is only generic, your design will not be the same, so don't include my diagram expect as reference). What design styles you used and why. List of entity architecture pairs and the corresponding blocks in the block diagram. The code files and simulations results should also be submitted in the order that they appear in the list. The report should be neat and tidy. There should be a section in your write-up for each major building block. Index your entire report. Draw a diagram of the state machine that you generated, include description of each stage in the write-up and why is it necessary. Include timing information as necessary. Clearly mention the input and output signals from the state machine. Clearly mention which entity is each control output connected to and what functionality does it provide. Provide plots showing the functionality of your state machine, for each scenario of your design (i.e. read hit/ read miss/ write hit/ write miss). *This is going to be part of you final project report so make it nice looking (This is not a lab submission).*
6. A cover sheet should note the project name, course number, names of the students and sections. At the end include a sheet showing the breakup of work among the project partners.
7. A sample test bench and the correct output is provided on the webpage. Once your design is done and you have tested it with your own test benches, run this test case on your design. Include the output file from your design as well as the plots generated using SimVision. Example of how the waveforms should be plotted are provided on the webpage. Zoom into various sections of the plot before printing to make them clear. The test bench will only access the final inputs and outputs from the chip. However, the port names that you use in your top level chip entity might be different. Change the component instantiation segment of the test bench to match your design. Don't change anything else in the test bench. It is designed to check that your design follows proper timing. We will run additional test benches during our grading, so make sure that your circuit works according to the specifications.

8. Make a tar file containing all the code that you have written (includes design vhdl file, test vhdl files, input and output files). This should be created from the vhdl run directory. The command is
   *tar -cvf project_sub1.tar **
   Zip the tar file using the command
   gzip project_sub1.tar
   The submission directory is *proj_sub1*. There should be only one tar file per project group and it should contain all the code that you have mentioned in your report. Also submit a single pdf file for your report. Also make sure that you include in you report notes for the TA on how to run the simulations. i.e. which test file is used to simulate which circuit. What should be the format of the input file and what is the output format. The TA will run the simulations. If there are errors in your code you will loose points.

Late submission is not allowed (You will get a grade of 0 for the whole project if you miss any project submission deadlines so submit a report for whatever code you have working).