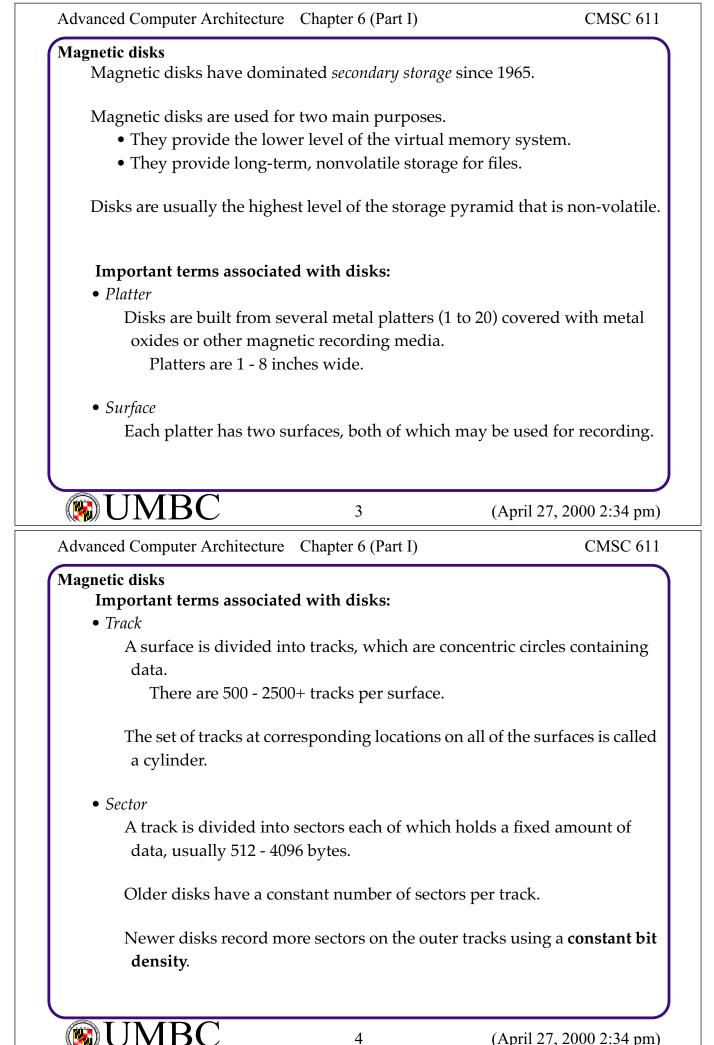
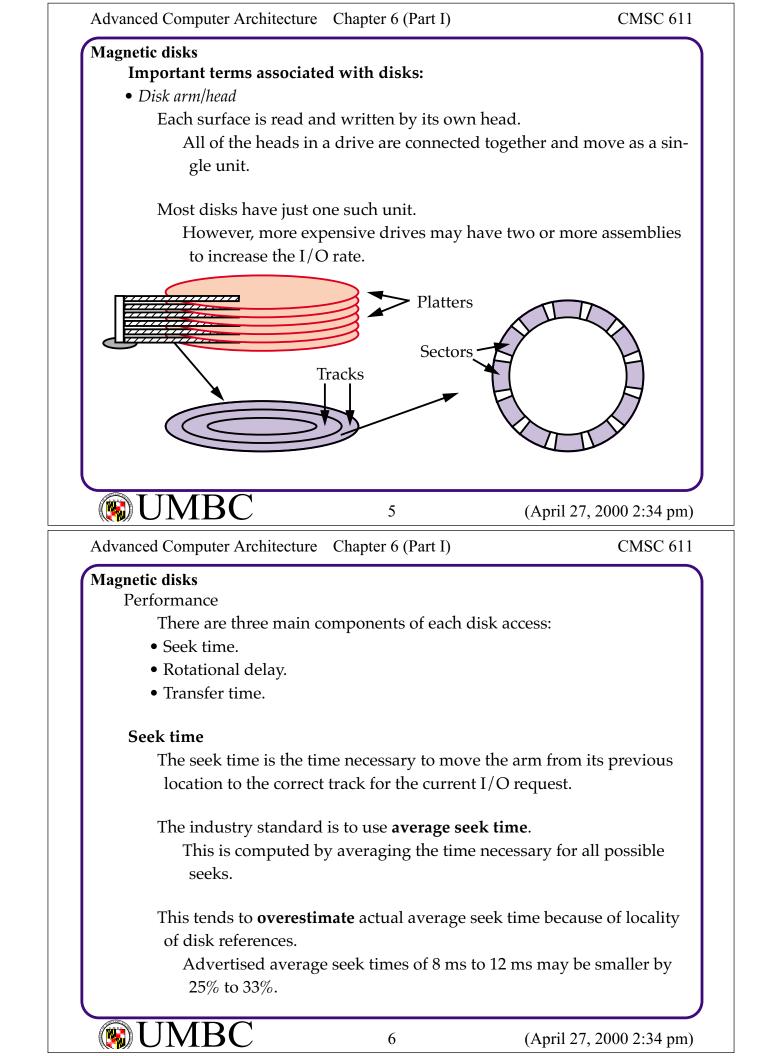
	er 6 (Part I)	CMSC 611
Why is I/O so important? Remember Amdahl's Law: Speeding up part of the proble	em while largely ig	noring the rest leads to
diminishing returns. This means that focusing on t	he CPU will result	in larger fractions of
time spent on I/O.		
<b>Response time</b> versus <b>throughput</b> It can be argued that I/O spee environment.		n a multiprogrammed
If a process waits for a peri	pheral, run anothe	r task.
This is an argument that perfore response time does not matte		d as throughput and
This is hardly the case today w tive software.		U U
Response time is directly re	elated to productiv	ity.
<b>WMBC</b>	1	(April 27, 2000 2:34 pm)
Advanced Computer Architecture Chapte	er 6 (Part I)	CMSC 611
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Storage devices Storage devices are mechanical, so tions.		
<b>Storage devices</b> Storage devices are <b>mechanical</b> , so	they are subject to bin a disk at 100,000	real physical limita- ) RPM.
Storage devices Storage devices are mechanical, so tions. For example, it is not possible to sp	o they are subject to pin a disk at 100,000 hat we know of tod	real physical limita- ) RPM. ay would fly apart.
Storage devices Storage devices are mechanical, so tions. For example, it is not possible to sp A disk made of any material th These mechanical delays are far me	o they are subject to pin a disk at 100,000 hat we know of tod ore difficult to elim	real physical limita- ) RPM. ay would fly apart. inate than electronic
Storage devices         Storage devices are mechanical, so tions.         For example, it is not possible to sp A disk made of any material the These mechanical delays are far me delays.         Reducing the size of mechanicates the size of electronic circuits.         We will focus on storage devices of the size of electronic circuits.	o they are subject to pin a disk at 100,000 hat we know of tod ore difficult to elim cal devices is more	real physical limita- ) RPM. ay would fly apart. inate than electronic
<ul> <li>Storage devices</li> <li>Storage devices are mechanical, so tions.</li> <li>For example, it is not possible to sp A disk made of any material the These mechanical delays are far me delays.</li> <li>Reducing the size of mechanication the size of electronic circuits.</li> <li>We will focus on storage devices of Magnetic disks.</li> <li>Magnetic tapes.</li> </ul>	o they are subject to pin a disk at 100,000 hat we know of tod ore difficult to elim cal devices is more	real physical limita- ) RPM. ay would fly apart. inate than electronic
Storage devices         Storage devices are mechanical, so tions.         For example, it is not possible to sp A disk made of any material the These mechanical delays are far me delays.         Reducing the size of mechanication the size of electronic circuits.         We will focus on storage devices of Magnetic disks.	o they are subject to pin a disk at 100,000 hat we know of tod ore difficult to elim cal devices is more	real physical limita- ) RPM. ay would fly apart. inate than electronic
<ul> <li>Storage devices</li> <li>Storage devices are mechanical, so tions.</li> <li>For example, it is not possible to sp A disk made of any material the These mechanical delays are far me delays.</li> <li>Reducing the size of mechanicates of the size of electronic circuits.</li> <li>We will focus on storage devices of Magnetic disks.</li> <li>Magnetic tapes.</li> <li>CD-ROMS.</li> </ul>	o they are subject to pin a disk at 100,000 hat we know of tod ore difficult to elim cal devices is more	real physical limita- ) RPM. ay would fly apart. inate than electronic



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(April 27, 2000 2:34 pm)



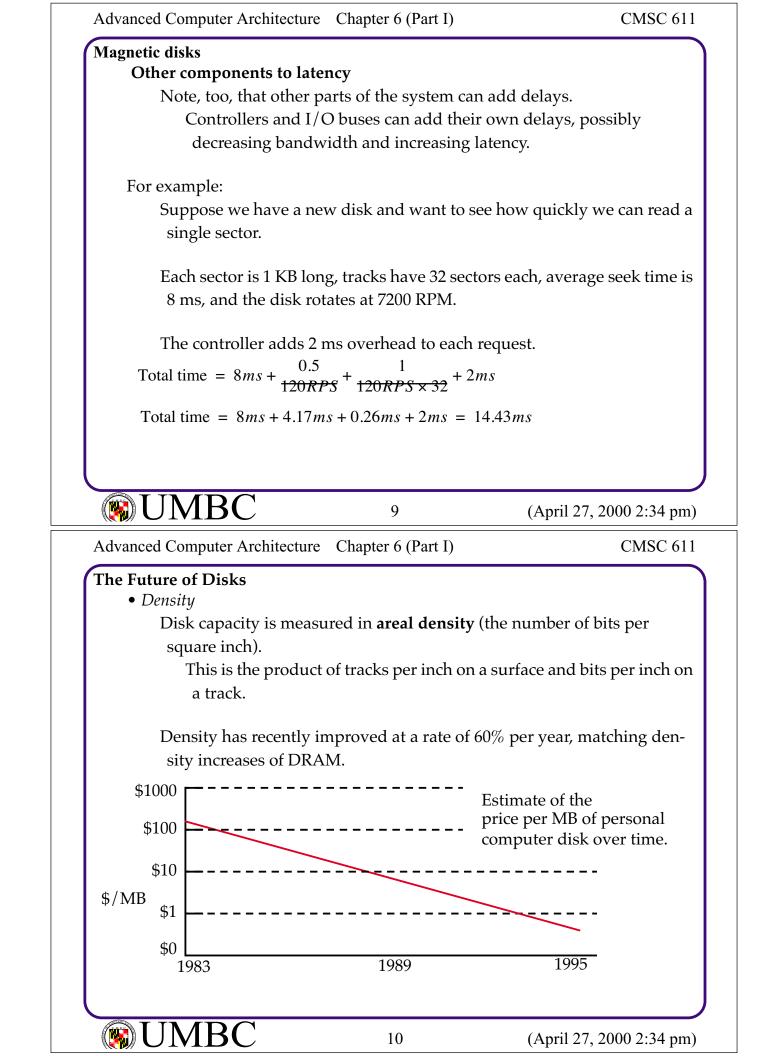
Advanced Computer Architecture Chapter 6 (Part I)	CMSC 611
Magnetic disks	
Rotational delay	
The time necessary for the requested sector to rotat	te under the head.
Most disks rotate at 3600 - 7200 RPM (note that dis RPM in 1975!).	ks rotated at 3600
On average, the disk must rotate <i>halfway</i> around to tor.	get to a desired sec-
On a disk rotating at 6000 RPM, this delay is 0.5 ms/min) = 5 ms.	/ (6000 RPM / 60,000
Therefore, the two mechanical components, movin waiting for the data to rotate under the head, add	-
Some disks can <b>read data out of order</b> into a buffer delay for a large transfer.	r, reducing rotational
A full track can be transferred in one rotation re I/O actually starts.	egardless of where the
WUMBC 7 (1	April 27, 2000 2:34 pm)
Advanced Computer Architecture Chapter 6 (Part I)	CMSC 611
Magnetic disks	
Transfer time	
The transfer time is the time it takes to read or writ	te a sector.
For the disk, this is approximately equal to the time	e it takes for the sector
to <i>pass fully</i> under the read/write head.	
It is a function of the block size, rotation speed, in the speed of the electronics.	recording density and
Typical rates in 1995 were 2 to 8 MB/sec.	
A disk rotating at 6000 RPM with 64 sectors per tra	ick and 512 bytes per

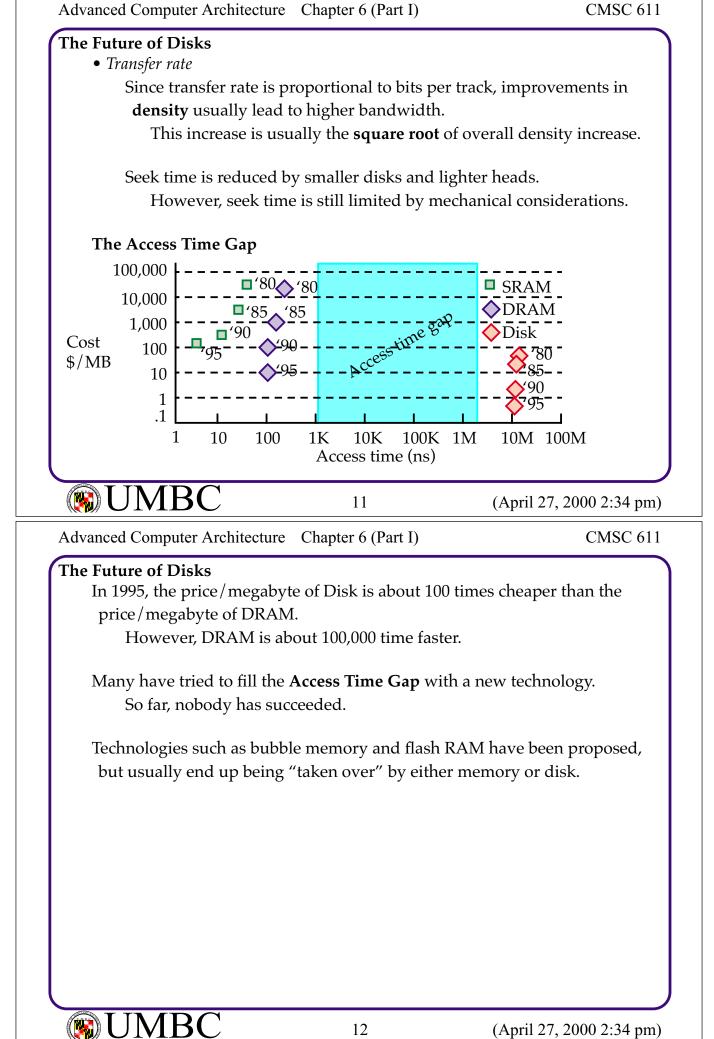
sector can read a **sector** in 10 ms/64 = 0.156 ms. Since 0.5 KB are transferred in this time, bandwidth is 3.2 KB/ms, or 3.2 MB/s.

Note that the transfer rate is higher for sectors on outside tracks (on disks that have variable number of sectors per track.)

8

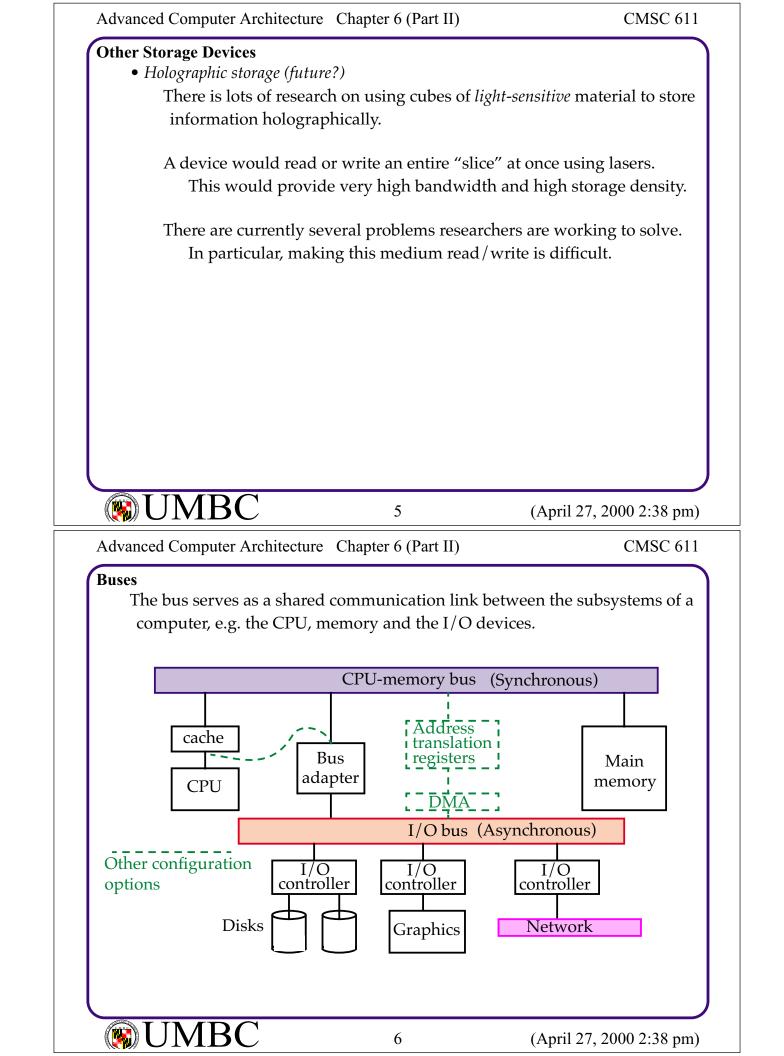
(**PR**) |





Advanced Computer Architect	ure Chapter 6 (Part II)	CMSC 611
Other Storage Devices		
A challenger to magnet	ic disks.	
• Optical disks (CDs)		
Optical disks conta	in data stored optically r	ather than magnetically.
Optical storage is r	emovable and inexpensiv	ve to manufacture.
For example, it	costs \$1 to \$2 per 500MB	CD-ROM.
CDs are a popular	medium for the distribut	ion of software.
Optical disks are us	sually write-once.	
-	alled <b>WORM</b> (Write Once	e Read Many) storage
They are also ee		c, neua many) storage.
Agreement on stan	dards for CDs have slow	ed their time-to-market,
e	c disks to stay ahead.	,
0 0	J	
However, writable	optical disks may have t	he potential to compete with
new tape technolo	gies for archival storage.	
<b>WMBC</b>	1	(April 27, 2000 2:38 pm)
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Advanced Computer Architect		
Advanced Computer Architecto <b>Other Storage Devices</b> • Magnetic tapes	ure Chapter 6 (Part II)	CMSC 611
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Advanced Computer Architectr <b>Other Storage Devices</b> • <i>Magnetic tapes</i> Magnetic tapes use	ure Chapter 6 (Part II)	CMSC 611
Advanced Computer Architectr <b>Other Storage Devices</b> • <i>Magnetic tapes</i> Magnetic tapes use netic disks. The major difference	ure Chapter 6 (Part II)	CMSC 611 ecording technology as mag-
Advanced Computer Architectr <b>Other Storage Devices</b> • <i>Magnetic tapes</i> Magnetic tapes use netic disks. The major difference • For tapes, the read	ure Chapter 6 (Part II) e the same basic kind of r	CMSC 611 ecording technology as mag- uch magnetic tapes.
Advanced Computer Architect <b>Other Storage Devices</b> • <i>Magnetic tapes</i> Magnetic tapes use netic disks. The major difference • For tapes, the read • For disks, they <i>floa</i>	ure Chapter 6 (Part II) e the same basic kind of rece: I/write heads actually to at above the disk surfaces	CMSC 611 ecording technology as mag- uch magnetic tapes. s (the Bernoulli effect).
Advanced Computer Architecto <b>Other Storage Devices</b> • <i>Magnetic tapes</i> Magnetic tapes use netic disks. The major difference • For tapes, the read • For disks, they <i>floa</i> Tapes are cheaper t	ure Chapter 6 (Part II) e the same basic kind of rece: I/write heads actually to at above the disk surfaces than disks for two reason	CMSC 611 ecording technology as mag- uch magnetic tapes. s (the Bernoulli effect).
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Advanced Computer Architect <b>Other Storage Devices</b> • <i>Magnetic tapes</i> Magnetic tapes use netic disks. The major difference • For tapes, the read • For disks, they <i>floa</i> Tapes are cheaper t • They pack more m • They are removab This means that a 9	ure Chapter 6 (Part II) e the same basic kind of rece: l/write heads actually to at above the disk surfaces than disks for two reason hedium into a fixed size b le (allowing one reader to	CMSC 611 ecording technology as mag- uch magnetic tapes. s (the Bernoulli effect). as: by recording on long strips. o access multiple tapes). as than \$20.
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CMSC 61
es or optical disks)
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nit of storage as more
tion for drives and
r a full system.



Buses	CMSC 611
Bus advantages:	
• They are <i>low cost</i> .	
A single set of wires is used to connect multip	le components.
• They are <i>versatile</i> .	
New devices can be easily added or removed.	
Disadvantage:	
• They create a <i>communication bottleneck</i> , possibly 1	imiting I/O throughput.
Two types:	
• CPU-memory buses	
Short, generally high speed and matched to m	aximize memory-CPU
bandwidth.	
• I/O buses	
Lengthy with many types of devices connecte	d to them, each of which
may have different data bandwidths.	
They usually follow a standard.	
ine, actuary renew a standard.	
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Advanced Computer Architecture Chapter 6 (Part II)	CMSC 611
- • • •	
Buses	
Buses	
<b>Buses</b> Basic bus transactions:	
<ul><li>Buses</li><li>Basic bus transactions:</li><li>If the transaction is a write (to memory), the data</li></ul>	n may be sent immediately
<ul> <li>Buses</li> <li>Basic bus transactions:</li> <li>If the transaction is a write (to memory), the data after (or perhaps in parallel with) the address.</li> </ul>	n may be sent immediately
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<ul> <li>Buses</li> <li>Basic bus transactions:</li> <li>If the transaction is a write (to memory), the data after (or perhaps in parallel with) the address.</li> <li>For reads (from memory), there is usually a delay address is sent and the time the data is ready.</li> </ul>	n may be sent immediately y between the time the
<ul> <li>Buses</li> <li>Basic bus transactions:</li> <li>If the transaction is a write (to memory), the data after (or perhaps in parallel with) the address.</li> <li>For reads (from memory), there is usually a delay address is sent and the time the data is ready.</li> </ul>	n may be sent immediately y between the time the ncy.
<ul> <li>Buses</li> <li>Basic bus transactions:</li> <li>If the transaction is a write (to memory), the data after (or perhaps in parallel with) the address.</li> <li>For reads (from memory), there is usually a delay address is sent and the time the data is ready. This delay occurs because of the memory later Typical bus read transaction (on a synchronous bu</li> </ul>	n may be sent immediately y between the time the ncy. s):
<ul> <li>Buses Basic bus transactions: <ul> <li>If the transaction is a write (to memory), the data after (or perhaps in parallel with) the address.</li> <li>For reads (from memory), there is usually a delay address is sent and the time the data is ready. This delay occurs because of the memory later Typical bus read transaction (on a synchronous but Clock Put address out Memory) </li> </ul></li></ul>	n may be sent immediately y between the time the ncy. s): y put <u>s data out</u>
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<ul> <li>Buses Basic bus transactions: <ul> <li>If the transaction is a write (to memory), the data after (or perhaps in parallel with) the address.</li> <li>For reads (from memory), there is usually a delay address is sent and the time the data is ready. This delay occurs because of the memory later Typical bus read transaction (on a synchronous but Clock Put address out Memory) </li> </ul></li></ul>	n may be sent immediately y between the time the ncy. s): y put <u>s data out</u>
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<ul> <li>Buses Basic bus transactions: <ul> <li>If the transaction is a write (to memory), the data after (or perhaps in parallel with) the address.</li> <li>For reads (from memory), there is usually a delay address is sent and the time the data is ready. This delay occurs because of the memory later Typical bus read transaction (on a synchronous but Clock Put address out and deasert read Memory and deasert read </li> </ul></li></ul>	n may be sent immediately y between the time the ncy. s): y put <u>s data out</u>
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<ul> <li>Buses Basic bus transactions: <ul> <li>If the transaction is a write (to memory), the data after (or perhaps in parallel with) the address.</li> <li>For reads (from memory), there is usually a delay address is sent and the time the data is ready. This delay occurs because of the memory later Typical bus read transaction (on a synchronous but </li> <li>Clock Put address out and deasert read </li> <li>Address Data </li> </ul></li></ul>	n may be sent immediately y between the time the ncy. s): y put <u>s data out</u>
<ul> <li>Buses Basic bus transactions: <ul> <li>If the transaction is a write (to memory), the data after (or perhaps in parallel with) the address.</li> <li>For reads (from memory), there is usually a delay address is sent and the time the data is ready. This delay occurs because of the memory later Typical bus read transaction (on a synchronous but </li> <li>Clock Put address out Address Data </li> </ul></li></ul>	n may be sent immediately y between the time the ncy. s): y put <u>s data out</u>

Advanced Computer Architecture Chapter 6 (Part II)

#### Bus Design Decisions

Cost versus performance trade-offs:

Option	Better performance	Lower cost
Bus width	Separate address & data	Multiplex address & data
	lines (adv for writes)	lines
Number of bus lines	Wider is faster	Narrower is cheaper
Transfer size	Multiple words have less	Single word transfer has
	bus overhead	simpler logic
Bus masters	Multiple, arbitrated	Single, no arbitration
Split transaction	Yes. Separate request and	No. Continuous connec-
	reply packets get higher	tion is cheaper and has
	bandwidth	lower latency
Clocking	Synchronous	Asynchronous

The choice of using any of the options listed in the first three rows is straightforward.

All give higher performance at more cost.

# **WUMBC**

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(April 27, 2000 2:38 pm)

Advanced Computer Architecture Chapter 6 (Part II)

CMSC 611

## **Bus Options**

### **Bus masters**

A bus master is a device on the bus that has the power to initiate a transaction.

The CPU is always a bus master.

I/O devices can also be bus masters.

With multiple masters, an arbitration scheme is required to determine who gets the bus next.

## Split transactions

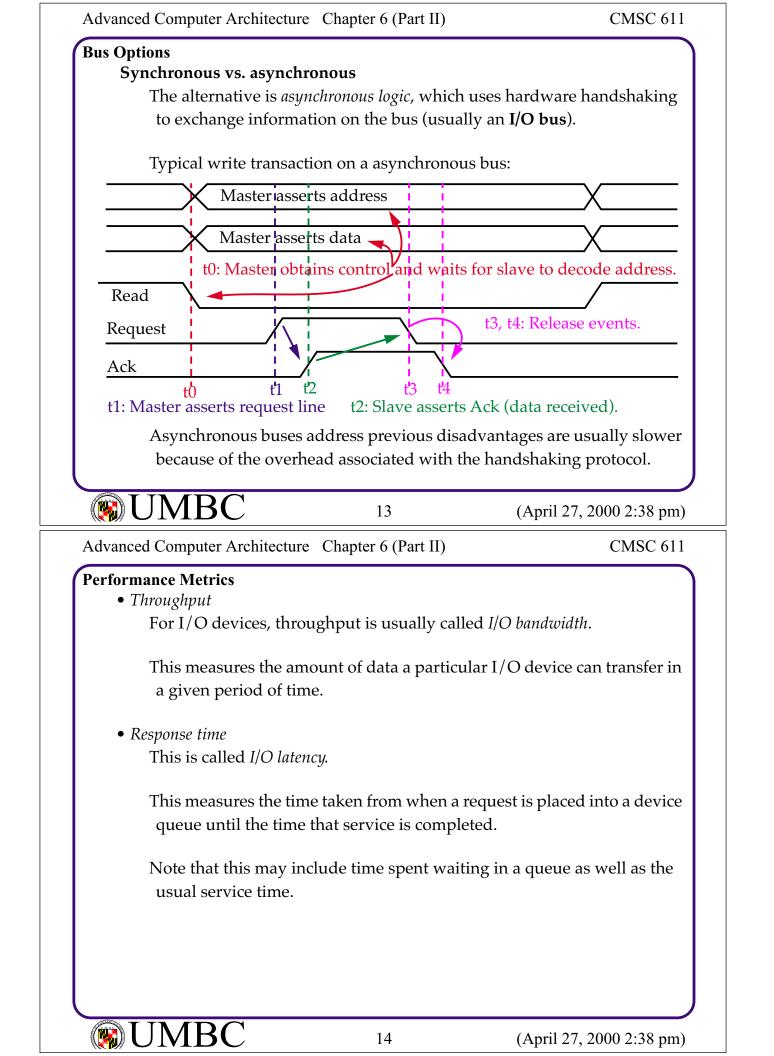
For many buses, a transaction must be performed atomically.

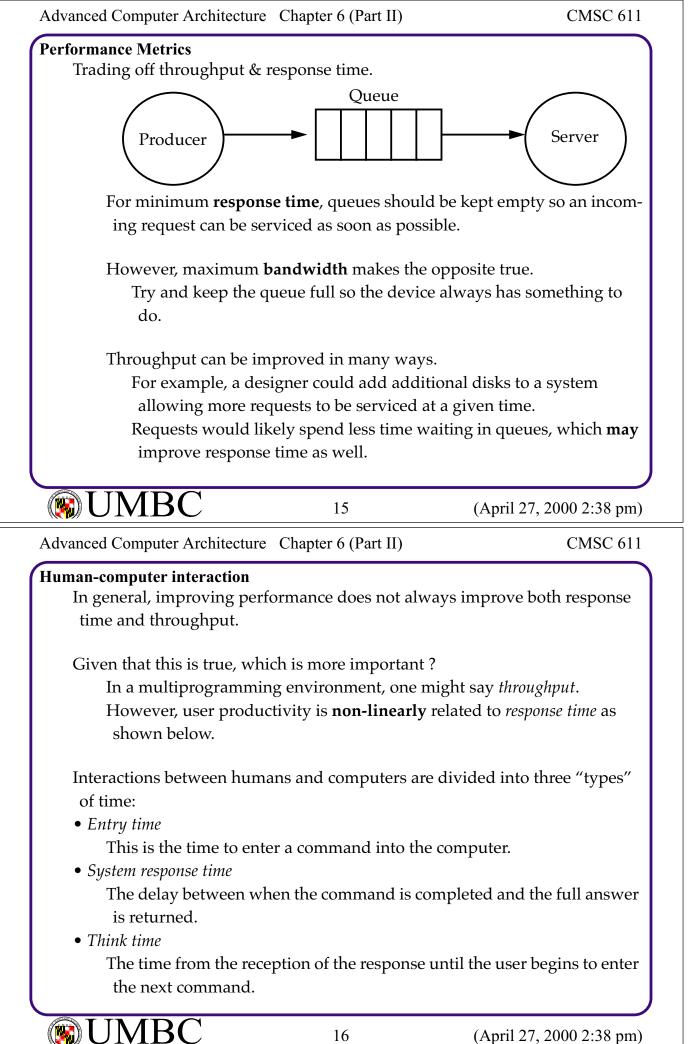
This means the bus is busy from the time the data is request until the time the request is complete.

This may work well for memory, but it can be intolerable for I/O where data may not be ready for 10ms after the request.



	ure Chapter 6 (Part II)	CMSC 61
Bus Options		
Split transactions		
•	-	plit transactions provide ar
improvement in b	andwidth.	
In a split transactio	on, the read request is sent a	and the bus is <i>released</i> while
the data is prepare	-	
Once memory h	nas retrieved the data, it ar	bitrates for the bus and
'tags' the data	reply for the CPU.	
This makes the bus	s available for other bus m	asters while memory reads
	e requested address.	usters while memory redus
Split transactions c	an be even more beneficia	l for I/O buses.
-	SCSI bus can have <b>several</b>	long disk transactions in
progress at the	e same time.	
However, a split tra	ansaction may have higher	<i>latency</i> than a bus that is
-	omplete transaction (due to	·
S UMBC	11	(April 27, 2000 2:38 pm
Advanced Computer Architect	ure Chapter 6 (Part II)	CMSC 61
Bus Options		
Synchronous vs. async		
Synchronous vs. async Synchronous buses	require a fixed protocol for	
Synchronous vs. async Synchronous buses		
<b>Synchronous vs. async</b> Synchronous buses tive to a global clo	require a fixed protocol for ock that all devices agree u	pon.
Synchronous vs. async Synchronous buses tive to a global clo Signals are only con	require a fixed protocol for ock that all devices agree u nsidered valid at certain p	pon.
Synchronous vs. async Synchronous buses tive to a global clo Signals are only con form (usually the s	require a fixed protocol for ock that all devices agree u nsidered valid at certain p rising or falling edge).	pon. oints on the clock wave-
Synchronous vs. async Synchronous buses tive to a global clo Signals are only con form (usually the If all devices are eq	require a fixed protocol for ock that all devices agree u nsidered valid at certain p	pon. oints on the clock wave-
Synchronous vs. async Synchronous buses tive to a global clo Signals are only con form (usually the s	require a fixed protocol for ock that all devices agree u nsidered valid at certain p rising or falling edge).	pon. oints on the clock wave-
Synchronous vs. async Synchronous buses tive to a global clo Signals are only con form (usually the If all devices are eq pensive and fast.	require a fixed protocol for ock that all devices agree u nsidered valid at certain p rising or falling edge). Jually "fast," synchronous	pon. oints on the clock wave-
Synchronous vs. async Synchronous buses tive to a global clo Signals are only con form (usually the If all devices are eq pensive and fast. Two disadvantages	require a fixed protocol for ock that all devices agree u nsidered valid at certain p rising or falling edge). Jually "fast," synchronous	pon. oints on the clock wave- works well and it is inex-
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Synchronous vs. async Synchronous buses tive to a global clo Signals are only con form (usually the If all devices are eq pensive and fast. Two disadvantages • Cheap devices, sur under the same f	require a fixed protocol for ock that all devices agree u nsidered valid at certain p rising or falling edge). qually "fast," synchronous s: ch as keyboards, must hav	pon. oints on the clock wave- works well and it is inex- re logic that is able to run ks.
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<sup>(</sup>April 27, 2000 2:38 pm)

